

UDC 62-501.001.11

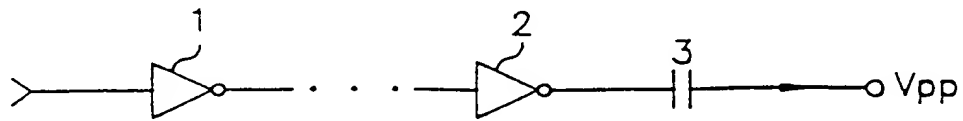


FIG. 1A

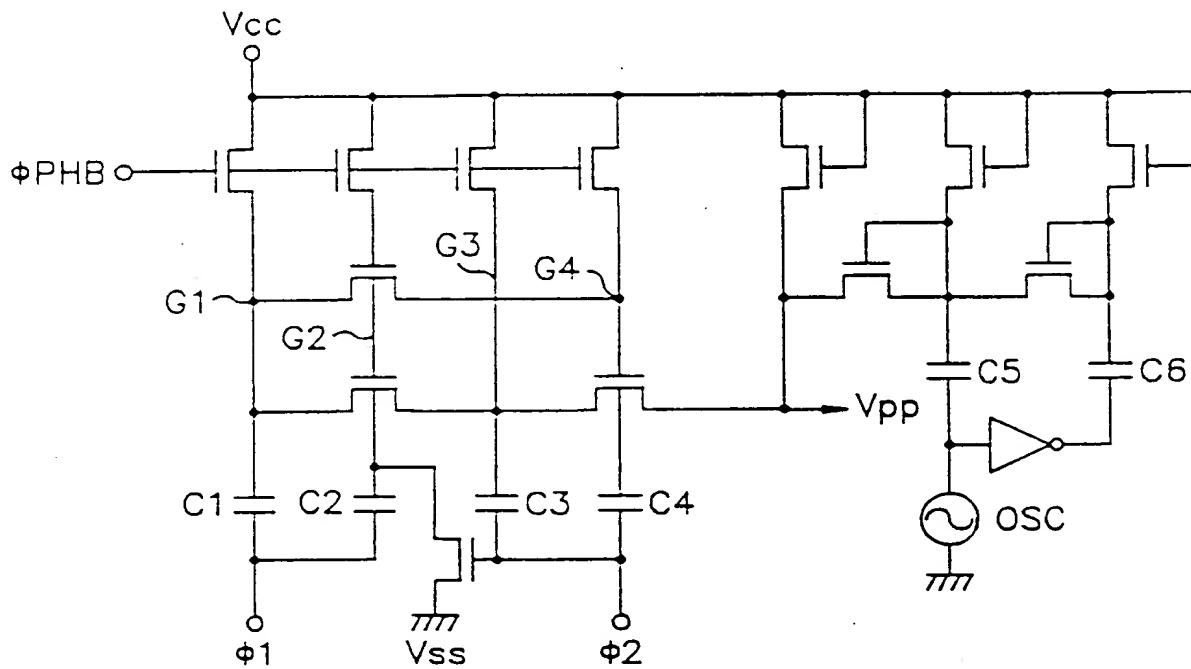


FIG. 1B

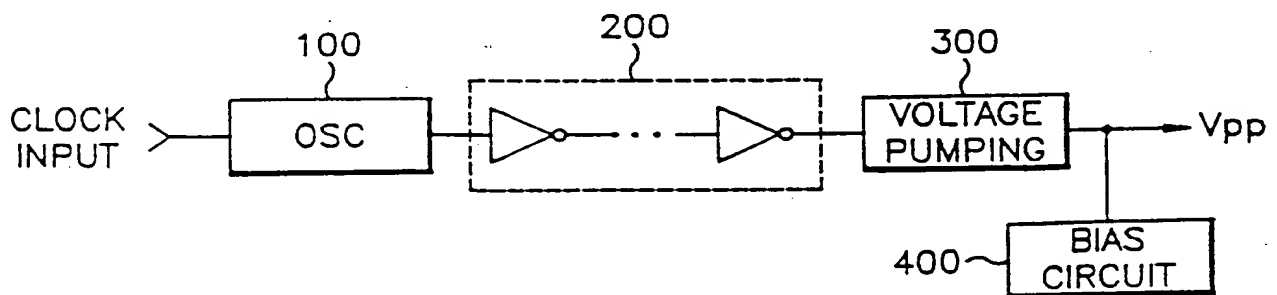


FIG. 2

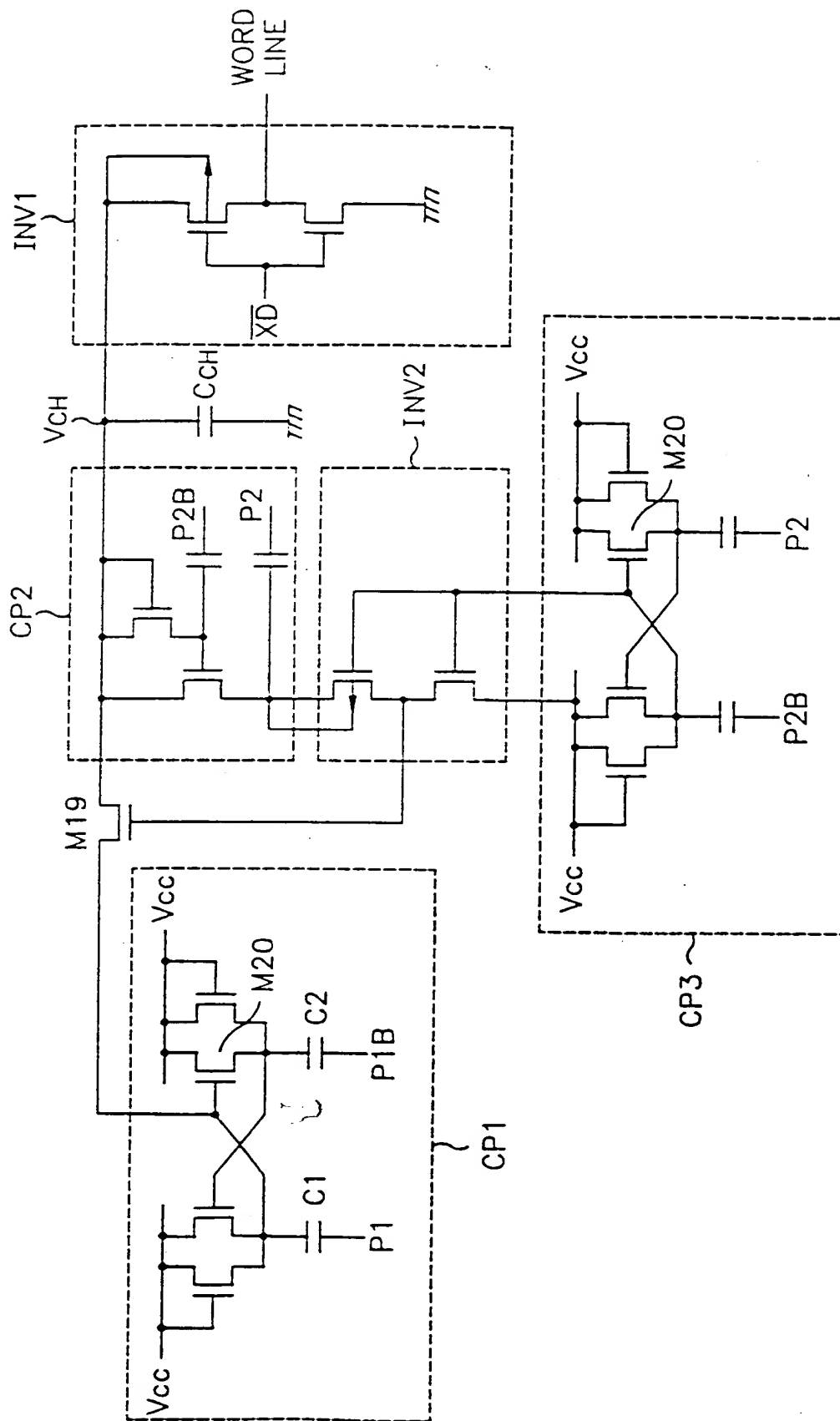


FIG. 1C



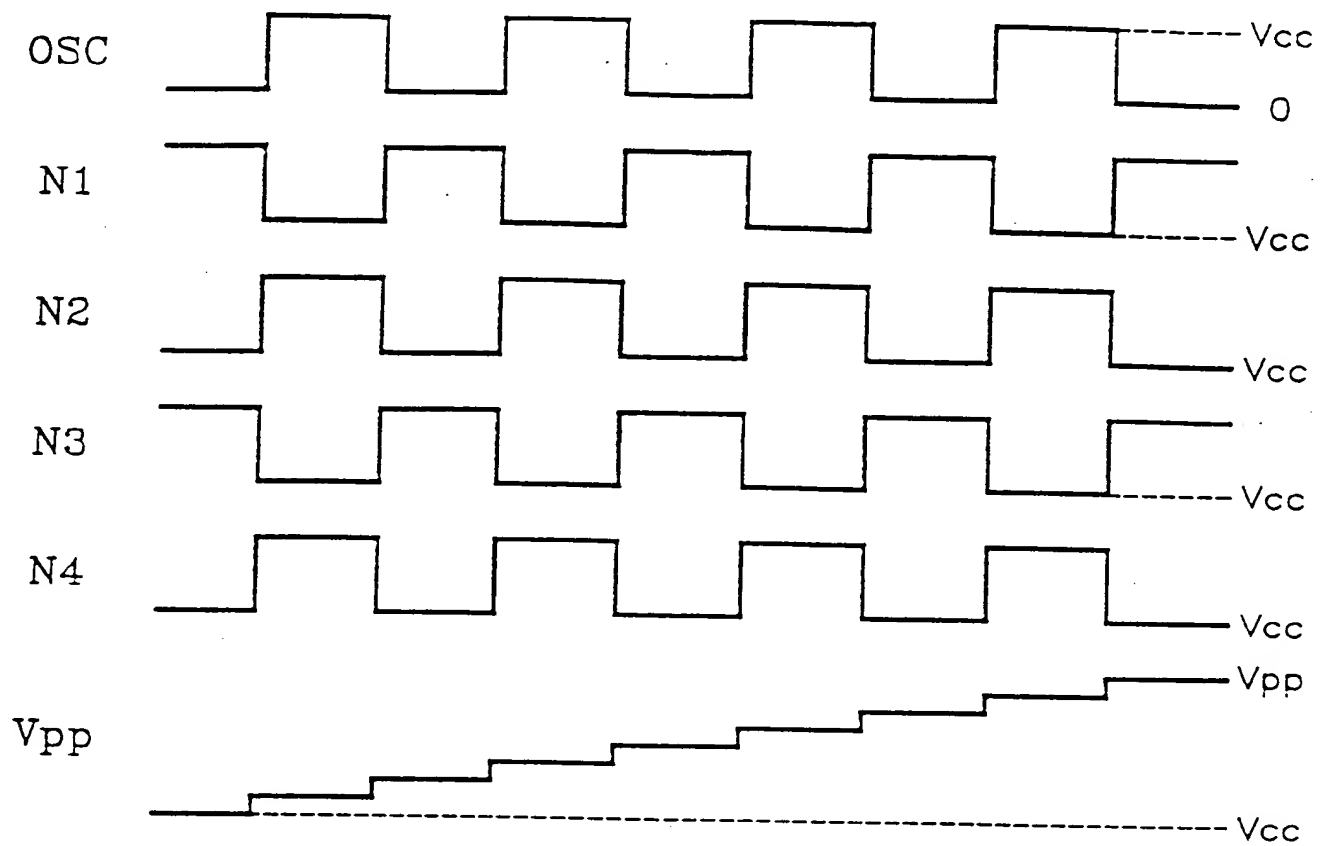


FIG. 3B

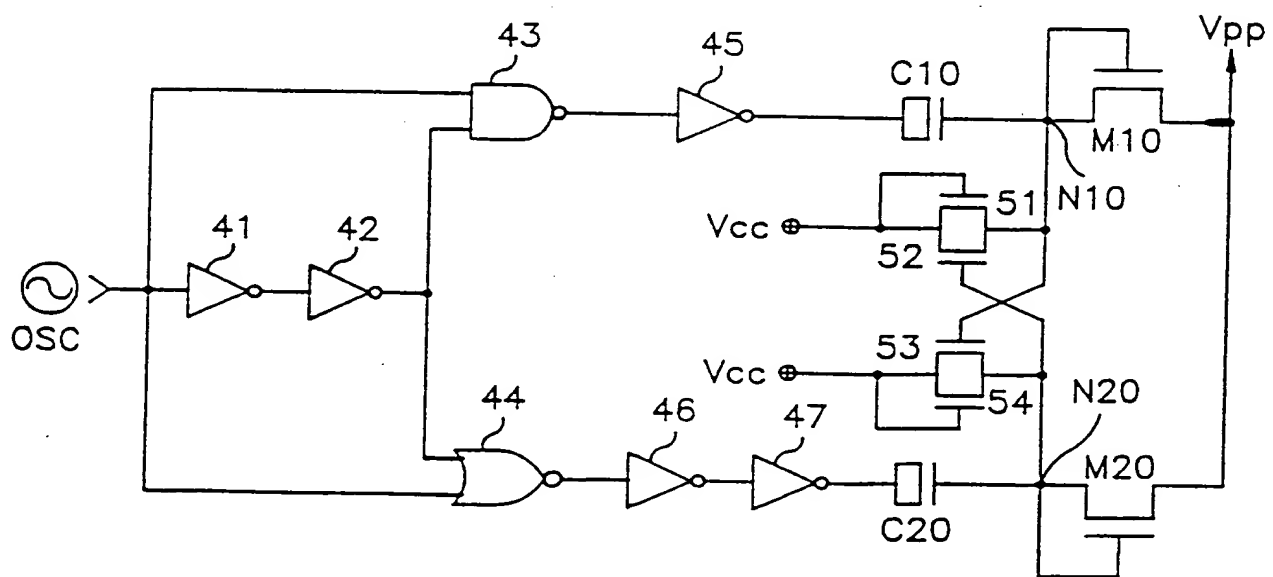


FIG. 3C

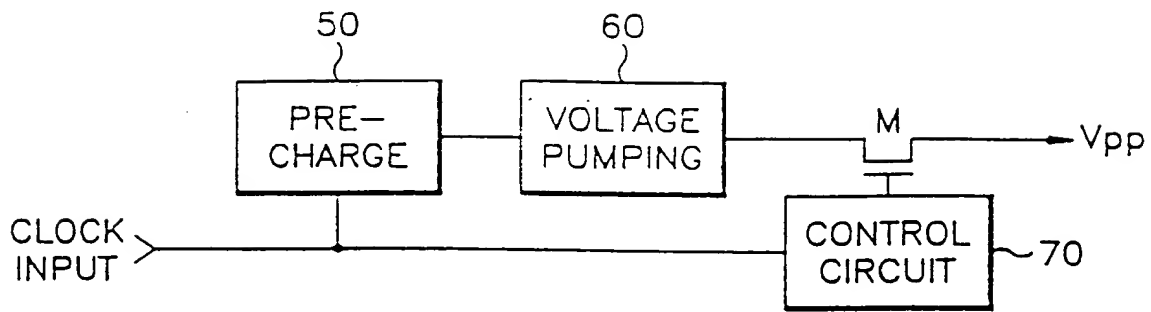


FIG. 4

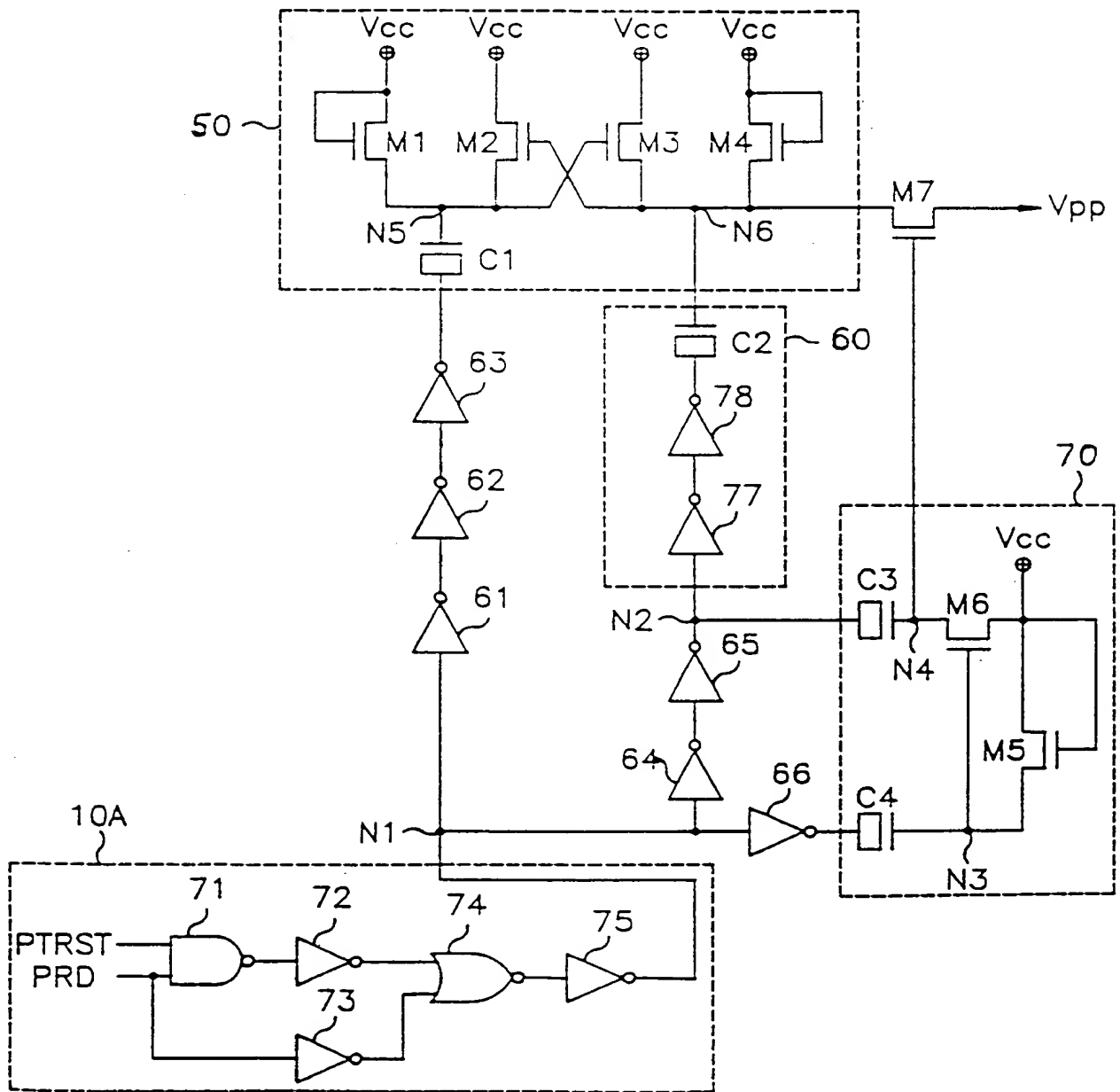
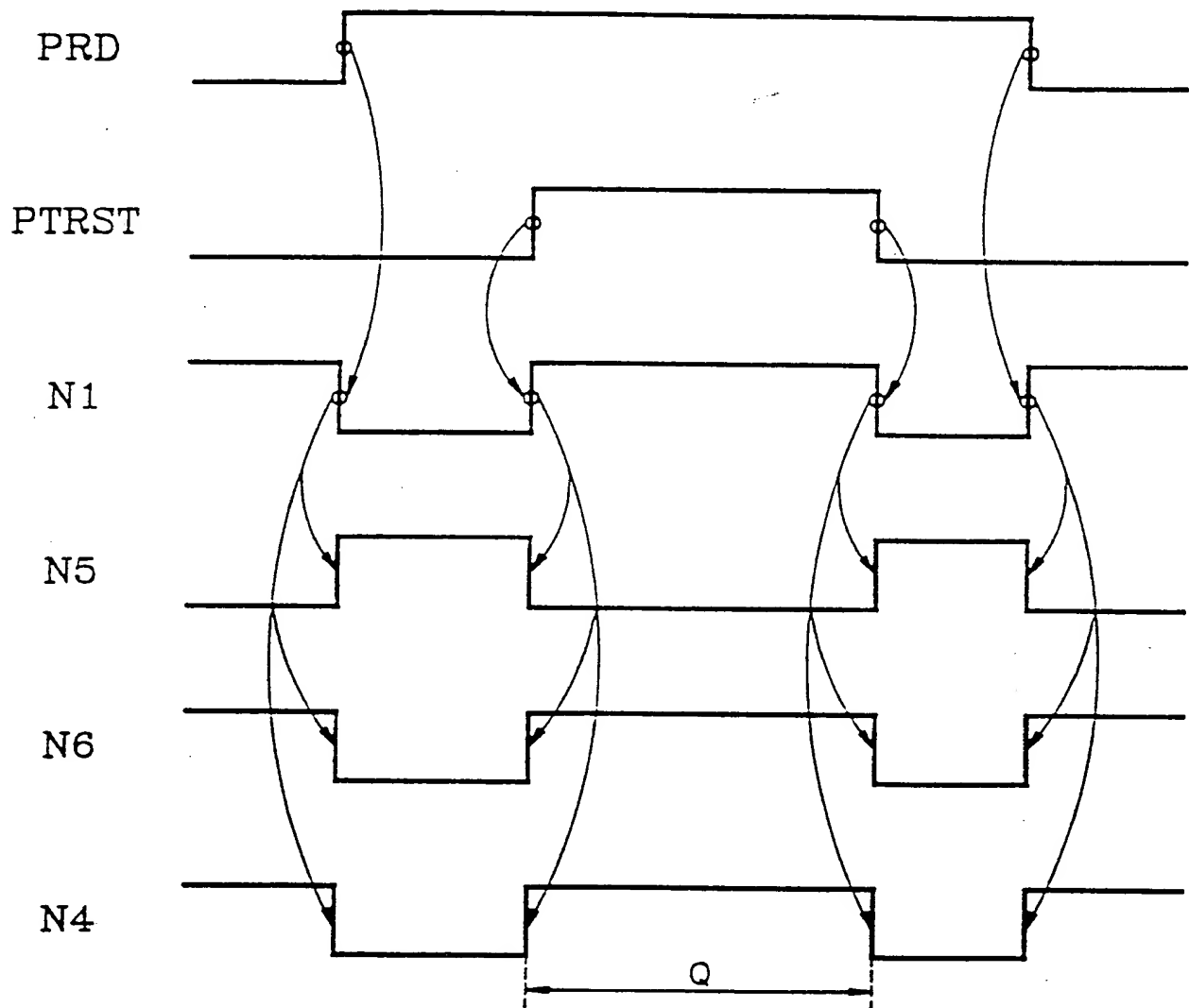


FIG. 5A

*FIG. 5B*

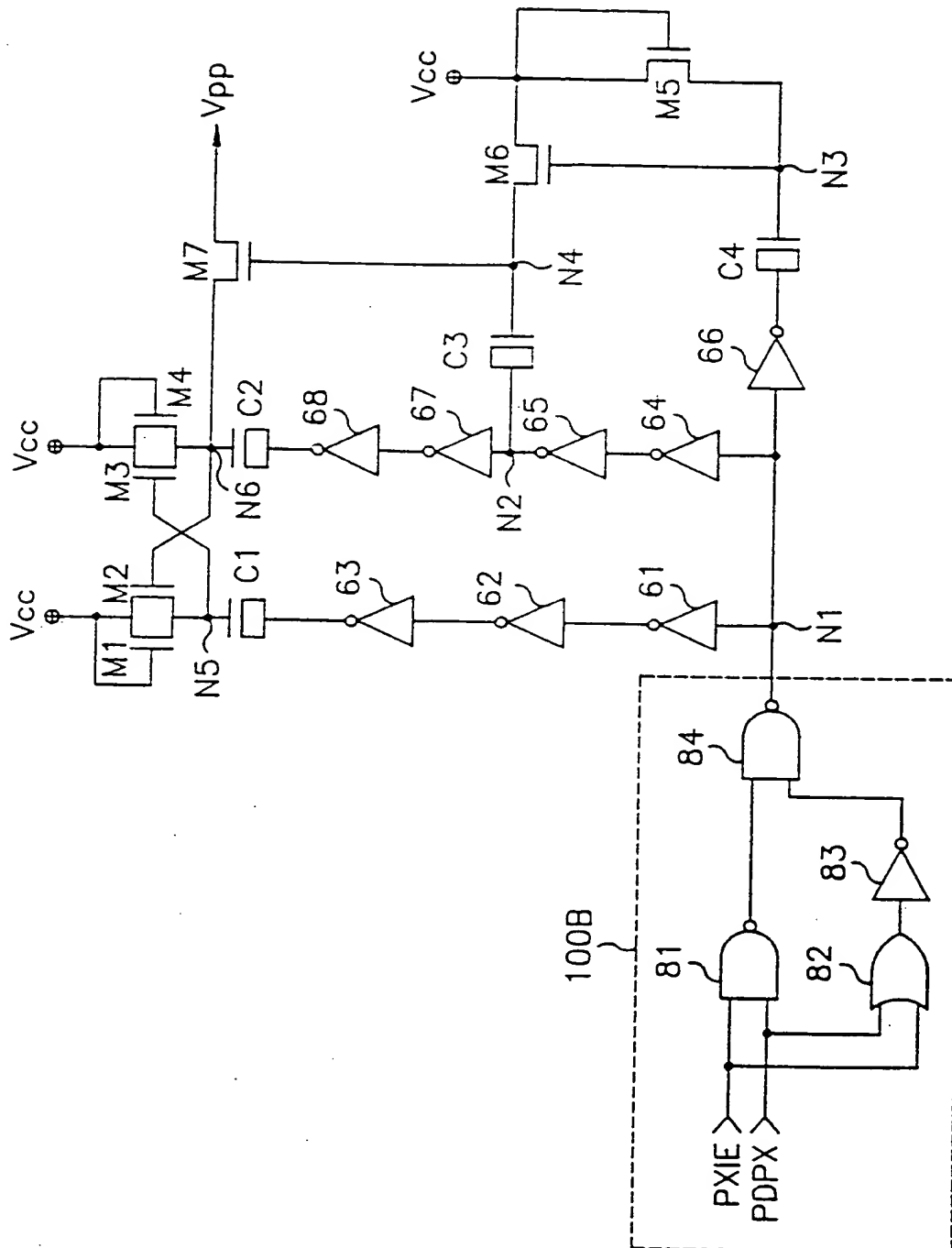
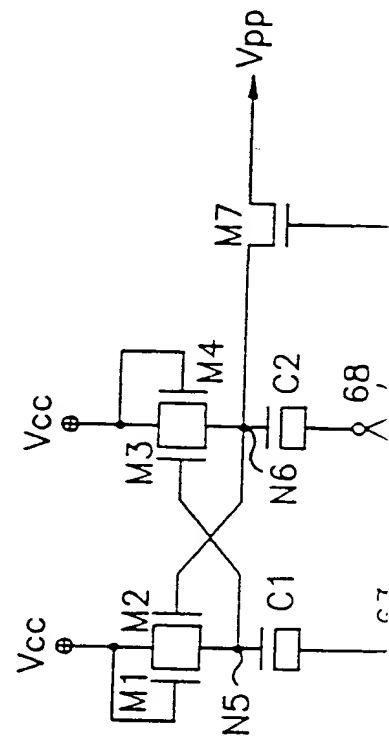


FIG. 5C





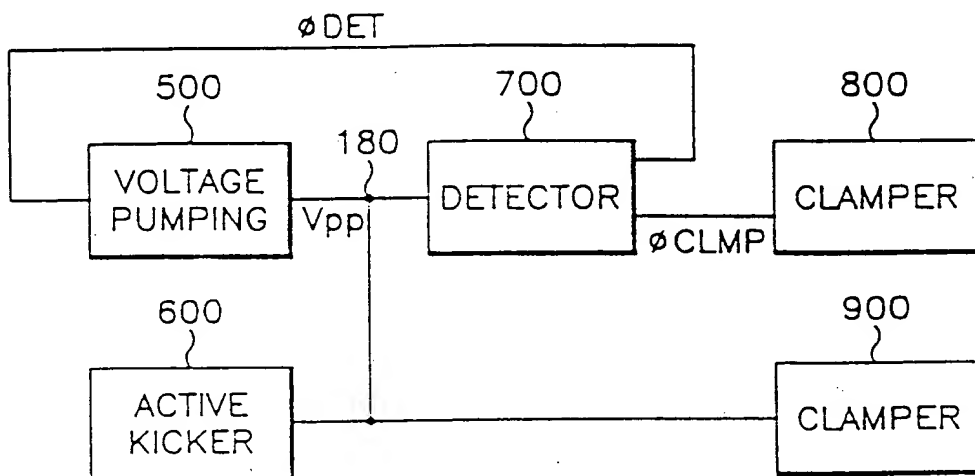


FIG. 6

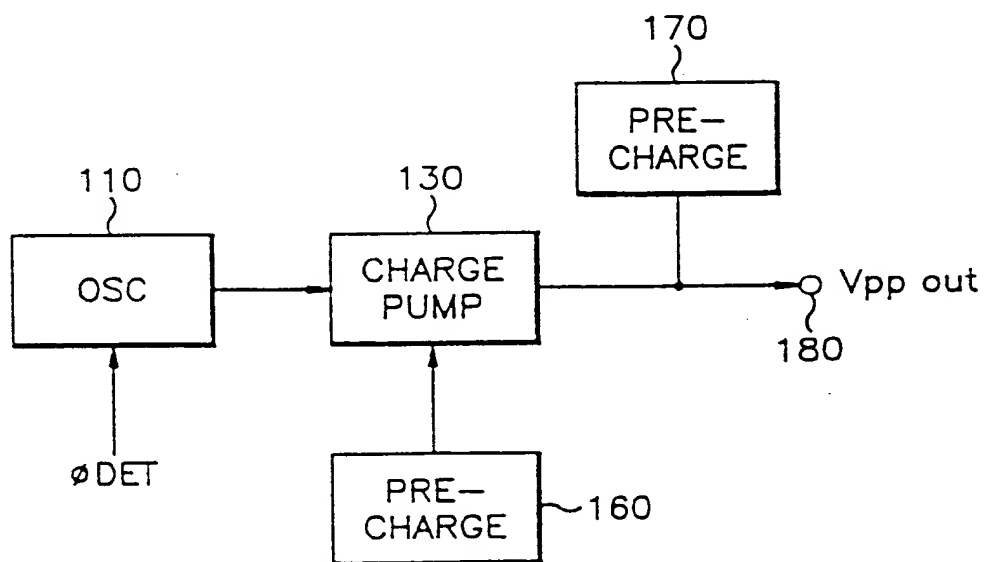


FIG. 7A

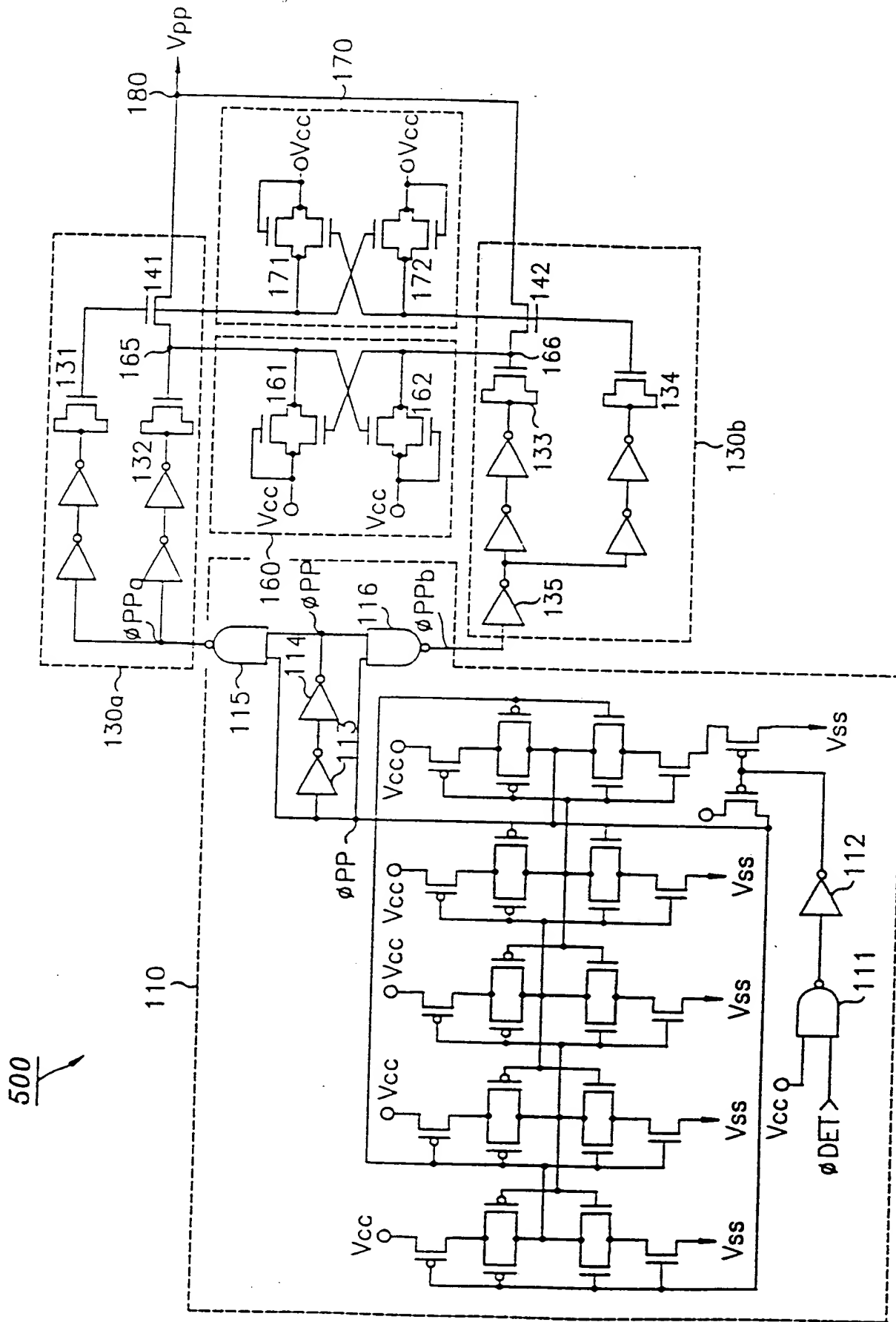


FIG. 7B

600

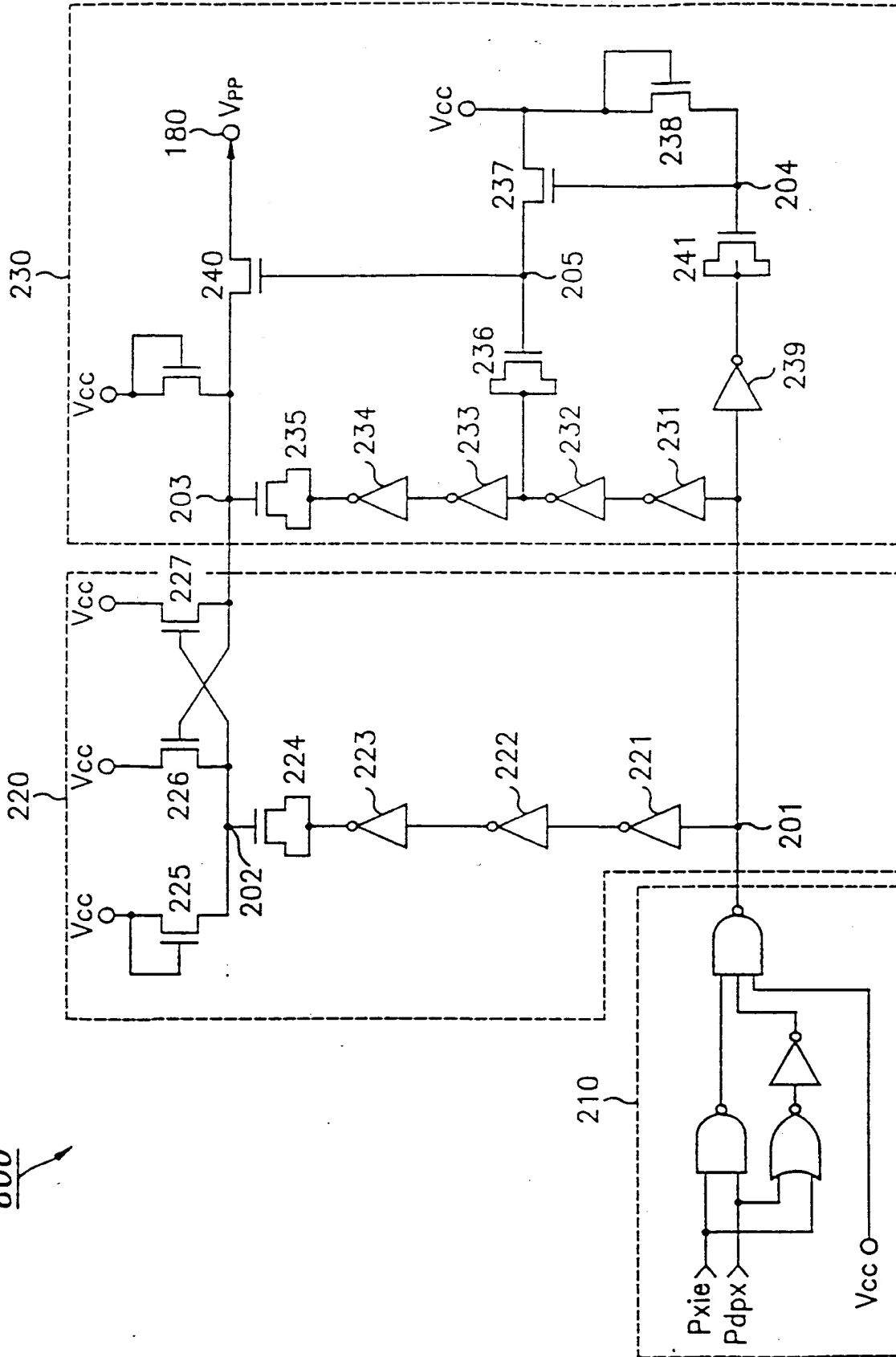


FIG. 7C

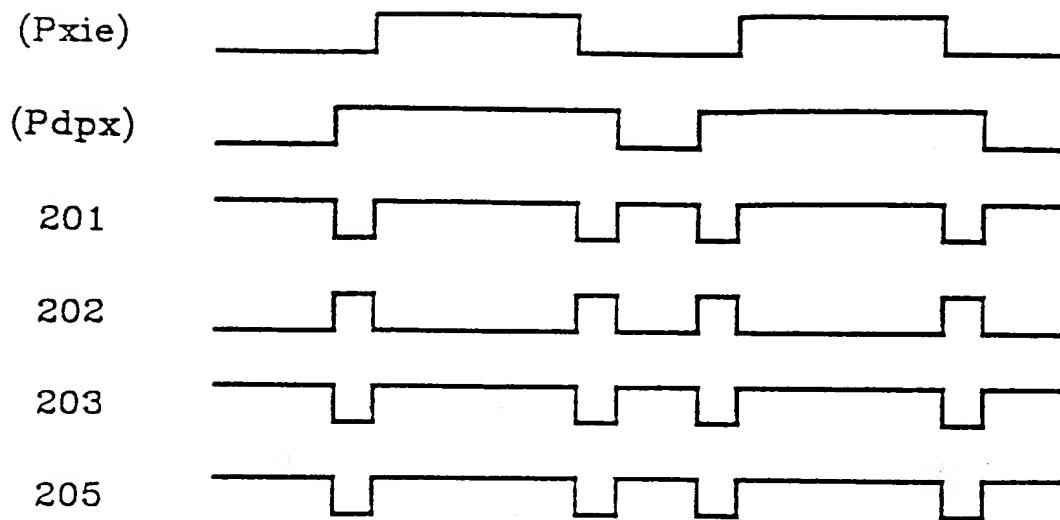


FIG. 7D

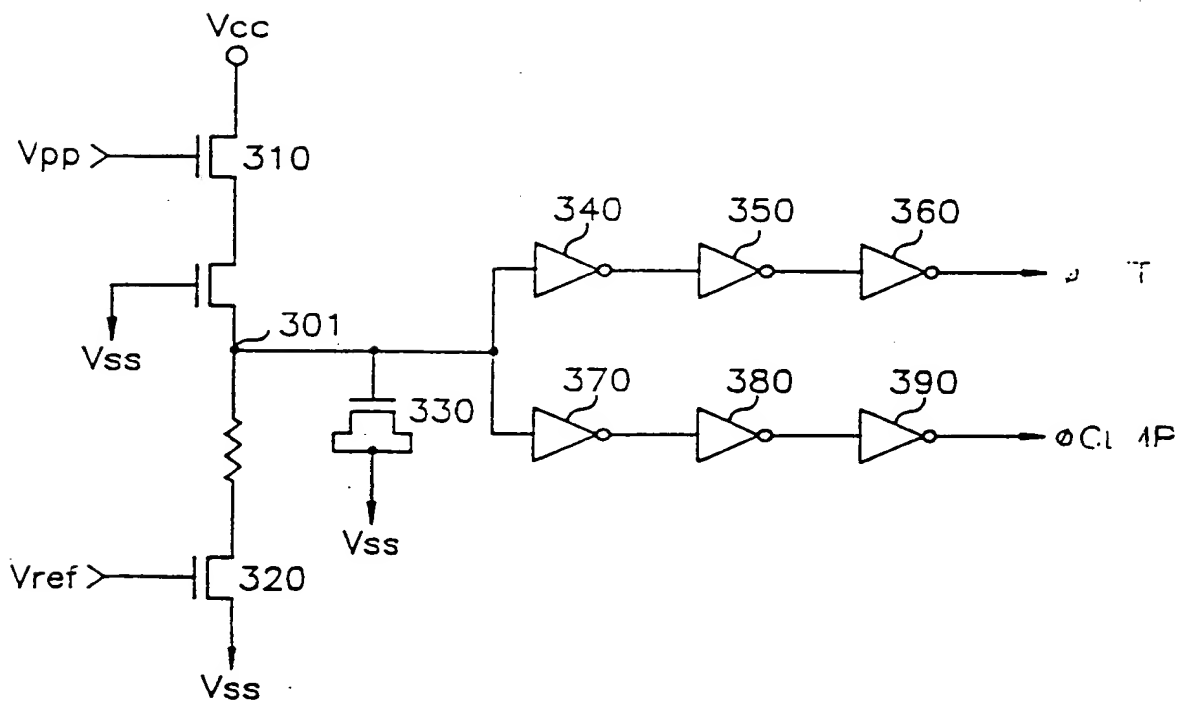


FIG. 7E

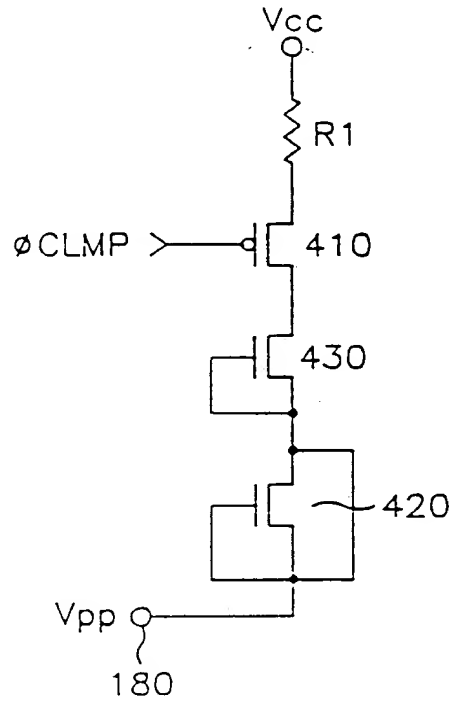
800, 900

FIG. 7F

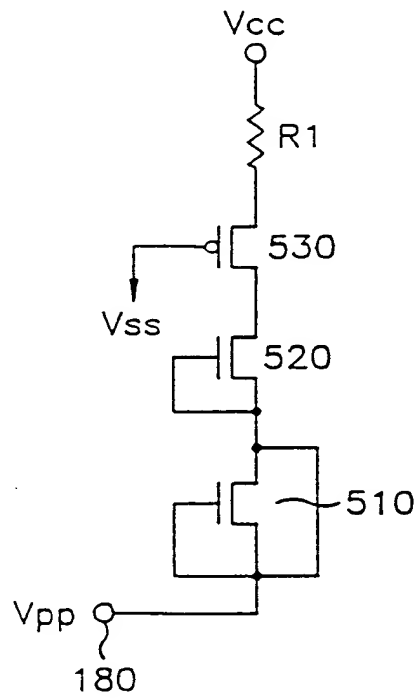
800, 900

FIG. 7G

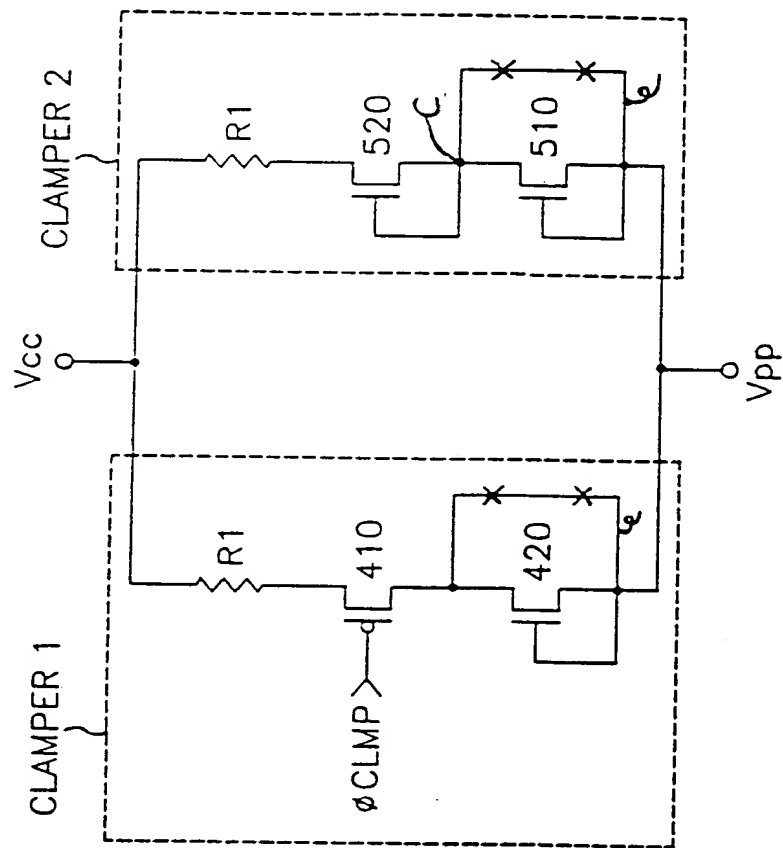


FIG. 7H

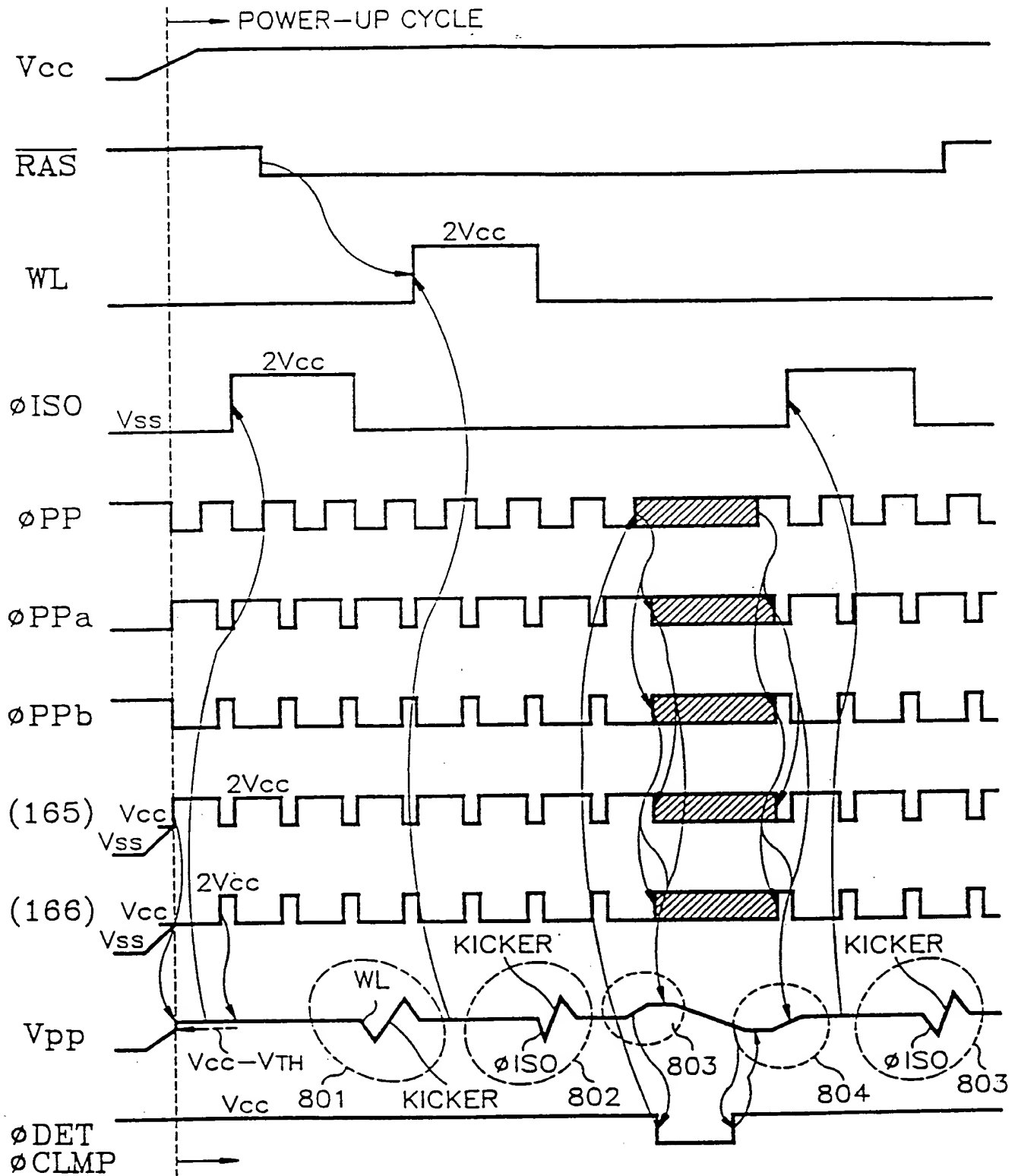


FIG. 8



## VOLTAGE PUMPING CIRCUITS

The present invention relates to voltage pumping circuits, and is concerned particularly, although not exclusively, with circuits for supplying  
5 a voltage to semiconductor memory devices of high complexity that require a low level source voltage.

The complexity of semiconductor memory devices has rapidly increased, so that memory devices with a capacity of several tens of mega bits  
10 (Mbit) are fabricated to design rules of 1-micron (micrometer) or less. Such semiconductor memory devices mostly comprise a plurality of CMOS elements, where the operating voltage is applied across thin dielectric films. As the complexity increases, the space between the CMOS elements or signal lines is reduced together with the thickness of the dielectric films, so that it  
15 is required to lower the level of the operating voltage. For example, memory devices of the order of 64Mbit usually have an operating voltage of 1.5V. However, if the operating voltage of the memory device is only lowered without considering other conditions, the voltage dropping caused by the threshold voltage of the MOS transistors and the resistances of signal lines  
20 during the transmission of data signals often makes it impossible to read and write data. In order to resolve this problem, an externally applied source voltage is amplified within the chip of the memory device. Such amplifying means is usually a called pumping circuit, bootstrapping circuit or voltage-raising circuit, and in the present application is referred to as a pumping  
25 circuit.

Referring to Figure 1A of the accompanying diagrammatic drawings for illustrating a conventional pumping circuit, enable clock pulses are applied

through a drive circuit 1, 2 to one electrode of a pumping capacitor 3, which provides at the other electrode a pumped voltage  $V_{pp}$  increased by coupling to a level greater than that of the voltage applied to the one electrode. Although this pumping circuit has a simple structure, there is no means provided for stabilizing the output of the pumping capacitor 3 and therefore its operational reliability decreases in memory devices of high complexity with a low operating voltage. Moreover it is difficult to adjust the timing of the enable clock pulses.

10 In order to improve the pumping circuit of Figure 1A, there has been proposed another voltage pumping circuit (see IEEE JOURNAL OF SOLID-STATE CIRCUIT, VOL.24, NO.3, JUNE 1989) as shown in Figure 1B of the accompanying diagrammatic drawings. In Figure 1B,  $\Phi_{PHB}$  represents a word line precharge signal,  $\Phi 1$  and  $\Phi 2$  clock signals to enable row address  
15 signals, and OSC an oscillator signal. When the chip is enabled on standby, i.e. precharging before and after performing a read/write operation, the word line precharge signal  $\Phi_{PHB}$  goes to  $V_{pp}$  level. In the operational mode of the chip, the signal  $\Phi_{PHB}$  is supplied with ground voltage level (0V).

20 As shown in Figure 1B, if the word line precharge signal  $\Phi_{PHB}$  is dropped from  $V_{pp}$  level to 0V, the clock signals  $\Phi 1$  and  $\Phi 2$  are raised to  $V_{cc}$  level. Then the clock signal  $\Phi 1$  causes the coupling effect of capacitors C1 and C2 to raise the voltages of the signal lines G1 and G2 to  $V_{cc}$  level or more, while the clock signal  $\Phi 2$  causes the coupling effect of capacitors C3  
25 and C4 to raise the voltages of the signal lines G3 and G4 to  $V_{pp}$  level greater than  $V_{cc}$  level. Thereafter the raised voltages of the signal lines G1 and G2 are dropped to 0V by the clock signal  $\Phi 2$ . The voltages of the signal lines G3 and G4 are the output  $V_{pp}$ . If the chip changes state from

operational mode to standby, the word line precharge signal  $\Phi_{PHB}$  is applied with  $V_{pp}$  level and therefore the output of the circuit of Figure 1B has  $V_{cc}$  level. The voltage of  $V_{pp}$  level is produced only when a given row address signal is applied as an active signal.

5

The circuit of Figure 1B resolves the problems associated with the unstable voltage of  $V_{pp}$  and the precise timing of the input signal, but results in other problems. Namely, the additional circuit means for generating the word line precharge signal  $\Phi_{PHB}$  and clock signals  $\Phi_1$  and  $\Phi_2$  are required, making it difficult to obtain a chip of high complexity. Moreover, the voltage  $V_{pp}$  is output when the row address signal is applied active, enabling the clock signals  $\Phi_1$  and  $\Phi_2$ , thereby degrading the operational speed of the chip. Additionally, the circuit of Figure 1B shows low value of the voltage pumping efficiency in semiconductor memory devices of the order of 16Mbit or 64Mbit.

10

15

Figure 1C of the accompanying diagrammatic drawings shows another conventional voltage pumping circuit, which has been proposed by Yoshinobu Nakakome, et al of the Japanese Hitachi Company in an article entitled "An Experimental 1.5-V 64Mbit DRAM", IEEE Journal of Solid State Circuits, Vol.26, No.4, April 1991, pp.465-472. This article discloses a word line driver circuit for preventing the word line voltage from being dropped by the threshold voltage of an access transistor. As shown in Figure 1C, the word line driver produces a pumped voltage  $V_{CH}$  of  $2V_{cc}$  level by the feedback operation of charge pump circuits CP1 and CP2 even when the chip is in a low operation voltage. This circuit has the following problems.

20

25

First, the capacitance of the capacitor  $C_{CH}$  connected to the node  $V_{CH}$  becomes so great that the area of the chip is increased. When a voltage of "high" level is transferred to a selected word line, charge sharing occurs between the capacitor  $C_{CH}$  and the capacitance component  $C_{WL}$  of the word line. This relationship may be expressed by the following Eq. (1):

$$C_{CH} \times V_{CH} = (C_{WL} + C_{CH}) \times V_{WL}$$
$$V_{WL} = [C_{CH} / (C_{WL} + C_{CH})] \times V_{CH} \dots\dots\dots (Eq. 1)$$

From the Eq. 1, it is preferable for the voltage  $V_{WL}$  of the word line to equal the pumped voltage  $V_{CH}$ . To this end, the capacitance  $C_{CH}$  should have a value great enough to ignore the capacitance  $C_{WL}$ . After charge sharing is effected, the voltage dropping of the node  $V_{CH}$  should be small to secure stable operation of the circuit in the next cycle. Hence, the capacitance  $C_{CH}$  should be great.

Second, in order to make the voltage of the selected word line "high", the voltage pumping circuit is kept working to charge the node  $V_{CH}$ , thus increasing the power consumption of the chip. Moreover, the continuous working of the voltage pumping circuit of Figure 1C may excessively increase the voltage of the node  $V_{CH}$  to destroy the adjacent transistors.

Preferred embodiments of the present invention aim to provide a voltage pumping circuit for raising the level of an externally applied voltage within a semiconductor memory device of high complexity with a low power consumption.

It is another aim to provide a voltage pumping circuit for raising the level of an externally applied voltage that enables a semiconductor memory device of high complexity to work at a high speed with a low power consumption.

5

It is a further aim to provide a voltage compensation circuit that immediately compensates for dropping of the output voltage of a voltage pumping circuit conventionally used in a semiconductor memory device of high complexity with a low power consumption.

10

It is still another aim to provide a voltage compensation circuit that continuously raises the source voltage to a given level to improve the working efficiency of a semiconductor memory chip of high complexity.

15

It is a further aim to provide a voltage pumping circuit that raises the level of an externally applied voltage within a semiconductor memory chip without increasing the chip size.

20

It is a further aim to provide a voltage pumping circuit that reduces the power consumption of a semiconductor memory device of high complexity.

25

According to one aspect of the present invention, a voltage pumping means used in a semiconductor memory device with an oscillator for generating pulses of a given waveform comprises an input means for responding to the pulses of the oscillator, voltage pumping means for producing a voltage raised to a given level in response to an output signal of the input means, and bias means for transforming the output signal of the

voltage pumping means to a source voltage level of a chip while powering the chip.

According to another aspect of the present invention, a semiconductor  
5 memory device with a voltage pumping node for receiving a voltage raised to  
a given level over an operating source voltage of the chip is provided with a  
voltage compensation circuit, which comprises an input means for receiving  
an enable signal, voltage pumping means for generating a raised voltage in  
response to the transition of an output signal of the input means, and output  
10 means for transferring the raised voltage of the voltage pumping means,  
wherein a voltage drop of the voltage pumping node is immediately  
compensated in active operation of the chip such as enabling and testing of the  
chip. In this case, the enable signal may represent various signals according  
to the operational modes of the chip and may be generated by a row address  
15 strobe (RAS) signal or column address strobe (CAS) signal.

According to a further aspect of the present invention, a semiconductor  
memory device with circuits using a raised voltage over a source voltage  
comprises a voltage pumping node connected with said circuits, a voltage  
20 pumping circuit for generating a pumping voltage of a given level during  
powering of the chip, isolation means for transferring the pumping voltage to  
the voltage pumping node, an active kicker for compensating for dropping of  
the pumping voltage in response to an output signal of said circuits, a detector  
for producing a detection signal in response to the voltage level of the voltage  
25 pumping node to feed it back at least to the voltage pumping circuit, and a  
clamper for dropping the raised voltage by the raised amount in response to  
the detection signal. The pumping voltage produced by the voltage pumping  
circuit may be precharged to the source voltage level, while the raised voltage

may be precharged to a level dropped by the threshold voltage of an isolation transistor from the source voltage. The voltage pumping circuit and active kicker may receive the source voltage as an input signal. The active kicker may transfer the raised voltage through another isolation transistor to the raised voltage using circuits, which isolation transistor transfers an internally prepared pumping voltage as the raised voltage to the raised voltage using circuits.

According to another aspect of the present invention, there is provided a semiconductor memory device arranged to be powered by a supply voltage, and comprising an oscillator for generating pulses, and a voltage pumping circuit for generating at an initial power-up state a first output voltage which is substantially identical to said supply voltage, and pumping an output voltage up to a second output voltage prior to or upon the semiconductor memory device being enabled in response to pulses output from said oscillator, said second output voltage being higher than said first output voltage.

A semiconductor memory device as above may further comprise a detector for detecting variation of the output of said voltage pumping circuit, whereby said voltage pumping circuit operates to control the pumping operation thereof in response to the detection so as to maintain the output at said second output voltage.

Preferably, said voltage pumping circuit comprises:

input means operating in response to the pulses output from said oscillator;

voltage pumping means for generating said second output voltage in response to the output of said input means; and

5 bias means for forcing at the initial power-up state the output of said voltage pumping circuit into said first output voltage.

Preferably, said input means receive the pulses output from said oscillator to generate a pair of complementary signals.

10 A semiconductor memory device as above may further comprise driving means for amplifying the output signals of said input means.

Preferably, said voltage pumping means comprise a plurality of capacitors each having first and second electrodes, said first electrodes being  
15 respectively coupled to the output signals of said driving means.

A semiconductor memory device as above may further comprise first and second transmission transistors for providing said second output voltage to an output terminal by means of a charge sharing occurring through  
20 channels thereof, gates and selected first terminals of the channels of said first and second transmission transistors being respectively coupled to the second electrodes of said capacitors.

Preferably, said first and second transmission transistors are  
25 alternatively turned-on and turned-off in response to the complementary signals output from said input means.

Preferably, said bias means comprise:



a first bias circuit for providing the supply voltage to said first terminals of the channels of said first and second transmission transistors; and

5 a second bias circuit for providing the supply voltage to the gates of said first and second transmission transistors.

Preferably, said first and second bias circuits in association with each other provide the output terminal with said first output voltage at the initial power-up state.

10

According to a further aspect of the present invention, there is provided a voltage pumping circuit being provided with a supply voltage, and an oscillator for generating pulses, and comprising:

15 input means operating in response to pulses generated by said oscillator;

voltage pumping means for pumping up the output of said input means to generate a pumped voltage in response to the output of said input means;  
20 and

bias means for providing an output terminal of said voltage pumping means with the supply voltage.

25 A voltage pumping circuit as above may further comprise a detector for detecting variation of the output voltage of said voltage pumping circuit, whereby said voltage pumping circuit operates to control the pumping

operation thereof in response to the detection so as to maintain the output voltage at said pumped voltage.

5 Preferably, said input means receive the pulses output from said oscillator to generate a pair of complementary signals.

Preferably, said voltage pumping means comprise a plurality of capacitors each having first and second electrodes, said first electrodes being respectively coupled to the output signals of said input means.

10

A voltage pumping circuit as above may further comprise first and second diode-connected transmission transistors for providing the output voltage of said voltage pumping means to an output terminal by means of a charge sharing occurring through channels thereof, gates and selected first  
15 terminals of the channels of said first and second transmission transistors being respectively coupled to the second electrodes of said capacitors.

Preferably, said first and second diode-connected transmission transistors are alternatively turned-on and turned-off in response to the  
20 complementary signals output from said input means.

Preferably, said bias means provide the first terminal of the channel of said first and second diode-connected transmission transistors with the supply voltage.

25

According to another aspect of the present invention, there is provided a voltage pumping circuit in a semiconductor memory device having an oscillator for generating pulses. the circuit comprising:

input means operating in response to pulses output from said oscillator;

driver means for amplifying the output signals of said input means;

5        voltage pumping means comprising a plurality of capacitors each having first and second electrodes, said first electrodes being respectively coupled to the output signals of said driver means;

10        bias means for forcing at an initial power-up state the output voltage of said voltage pumping means to the supply voltage level; and

transmission means coupled to the output of said voltage pumping means, for generating a pumped voltage.

15        Preferably, said input means receive the pulses output from said oscillator to generate a pair of complementary signals.

20        A voltage pumping circuit as above may further comprise a detector for detecting variation of the output of said voltage pumping circuit, whereby said voltage pumping circuit operates to control the pumping operation thereof in response to the detection so as to maintain the output voltage at said pumped voltage.

25        According to a further aspect of the present invention, there is provided a voltage pumping circuit for a semiconductor memory device, the circuit having a voltage pumping node to which a pumped voltage higher than a supply voltage is applied, and comprising:

input means for receiving an enable signal input;

voltage pumping means for generating said pumped voltage in response to the output of said input means; and

5

output means for supplying the pumped voltage of said voltage pumping means;

whereby if said pumped voltage decreases during an active operation mode of the semiconductor memory device such as an enable mode or a test mode of the semiconductor memory device, said pumped voltage is compensated by the lowered voltage.

10

A voltage pumping circuit as above may further comprise precharge means for precharging the output of said voltage pumping means to the supply voltage during disable of the voltage pumping circuit, so as to increase voltage pumping efficiency of said voltage pumping means.

15

Preferably, said voltage pumping circuit is enabled only for the active operation mode of the semiconductor memory device.

20

Preferably, said voltage pumping means comprise at least one voltage pumping capacitor responsive to the output of said input means.

25

Preferably, said precharge means comprise:

at least one voltage pumping capacitor responsive to the output of said input means; and

a plurality of pull-up transistors coupled between the voltage pumping capacitor and the pumped voltage output;

5 whereby an initial output voltage of said voltage pumping means is precharged to the supply voltage through the pull-up transistors during a non-active operation mode of the semiconductor memory device.

10 Preferably, said enable signal is a signal generated in association with row or column address strobe signals, or a signal generated upon a power-up of the semiconductor memory device.

According to another aspect of the present invention, there is provided a voltage pumping circuit for a semiconductor memory device, the circuit having a voltage pumping node to which a pumped voltage higher than a supply voltage is applied, and comprising:

15

input means for receiving an enable signal input;

20 voltage pumping means for generating said pumped voltage in response to the output of said input means;

precharge means coupled to the output of said input means, for precharging the output of said voltage pumping means to the supply voltage during a non-active operation mode of the semiconductor memory device;

25 output means for supplying the pumped voltage of said voltage pumping means during an active operation mode of the semiconductor memory device;  
and

output control means for controlling operation of said output means in response to the output of said input means.

5 Preferably, said voltage pumping means comprise:

a driver circuit coupled to the output of said input means; and

10 a first voltage pumping capacitor having first and second electrodes, the first electrode being coupled to the output of said driver circuit.

Preferably, said precharge means comprise:

15 a second voltage pumping capacitor having first and second electrodes, the first electrode being coupled to the output of said input means;

a first pull-up transistor with a gate connected to the supply voltage and a channel connected between the supply voltage and the second electrode of said second voltage pumping capacitor;

20 a second pull-up transistor with a gate connected to the output of said voltage pumping means and a channel connected between the supply voltage and the second electrode of said second voltage pumping capacitor;

25 a third pull-up transistor with a gate connected to the supply voltage and a channel connected between the supply voltage and the output of said voltage pumping means; and

a fourth pull-up transistor with a gate connected to the second electrode of said second voltage pumping capacitor and a channel connected between the supply voltage and the output of said voltage pumping means.

5            Preferably, said output control means comprise:

a third voltage pumping capacitor having first and second electrodes, the first electrode being connected to the output of said input means, and the second electrode being connected to a control terminal of said output means;

10

a fourth voltage pumping capacitor having first and second electrodes, the first electrode being connected to the output of said input means;

a fifth pull-up transistor with a gate connected to the supply voltage and a channel connected between the supply voltage and the second electrode of said fourth voltage pumping capacitor; and

15

a sixth pull-up transistor with a gate connected to the second electrode of said fourth voltage pumping capacitor and a channel connected between the second electrode of said third voltage pumping capacitor and the supply voltage.

20

Preferably, said enable signal is a signal generated in association with row or column address strobe signals, or a signal generated upon power-up of the semiconductor memory device.

25

According to a further aspect of the present invention, there is provided a voltage pumping circuit for a semiconductor memory device, the circuit comprising:

5        an input node for sensing transition of an enable signal input, for compensating for a voltage drop of a pumped voltage output from the voltage pumping circuit, comprising:

10        voltage pumping means for generating said pumped voltage in response to transition of the enable signal input at said input node;

15        precharge means coupled to said input node, for precharging the output of said voltage pumping means to a supply voltage during a non-active operation mode of the semiconductor memory device;

      output means for supplying the pumped voltage of said voltage pumping means during an active operation mode of the semiconductor memory device; and

20        output control means for controlling operation of said output means in response to the enable signal input at the input node.

25        Preferably, said enable signal is a signal generated in association with row or column address strobe signals, or a signal generated upon a power-up of the semiconductor memory device.



According to a further aspect of the present invention, there is provided a semiconductor memory device having electrical circuitry provided with a pumped voltage higher than a supply voltage, the device comprising:

5           a voltage pumping node coupled to the circuitry;

voltage pumping means for pumping up a voltage for a power-up cycle of the semiconductor memory device, to generate the pumped voltage;

10           isolation means for supplying the pumped voltage to said voltage pumping node in response to the pumped voltage;

active kicker means for compensating for a voltage drop of the pumped voltage in response to the signal output from the circuitry;

15

detecting means for feeding-back a sensing signal indicative of variation of the pumped voltage to said voltage pumping means; and

20           clamping means for receiving the sensing signal to clamp the pumped voltage to compensate for a voltage pull-up of the pumped voltage.

Preferably, said voltage pumping means comprise:

25           an oscillator for generating a pumping clock in response to states of the supply voltage and the sensing signal; and

first and second charge pumps having first and second pumping nodes, said first and second charge pumps each operating complementarily in response to the pumping clock.

5            Preferably, said isolation means comprise:

a first isolation transistor with a gate connected to the first pumping node and a channel connected between the first pumping node and the voltage pumping node; and

10

a second isolation transistor with a gate connected to the second pumping node and a channel connected between the second pumping node and the voltage pumping node.

15            A semiconductor memory device as above may further comprise precharge means for precharging the output of said first and second pumping nodes to a predetermined voltage.

20            A semiconductor memory device as above may further comprise means for precharging a voltage at the voltage pumping node to a predetermined voltage.

Preferably, said active kicker means comprise:

25            a logic combination circuit for receiving signals from the circuitry;

a kicking node;

a pre-kicker for setting a voltage at the kicking node to a first level when the output of the logic combination circuit is at a first state;

5 a kicking driver converting the voltage at the kicking node from said first level to a second level when the output of the logic combination circuit is at a second state; and

10 a third isolation transistor with a channel connected between the kicking node and the voltage pumping node, said third isolation transistor operating in response to the voltage at the kicking node.

15 Preferably, said clamping means comprise a DC current path controllable by the sensing signal, disposed in series between the pumped voltage and the supply voltage.

Preferably, said clamping means comprise a DC current path disposed in series between the pumped voltage and the supply voltage.

20 According to another aspect of the present invention, there is provided a voltage pumping circuit including voltage pumping means for supplying a pumped voltage to electrical circuitry and comprising:

25 first switching means connected between said voltage pumping means and the electrical circuitry, for supplying the pumped voltage to the electrical circuitry in response to the pumped voltage; and

second switching means comprising voltage kicking means, connected between input and output terminals of the electrical circuitry, for supplying

a kicked voltage output from the voltage kicking means to the electrical circuitry in response to the output of the electrical circuitry.

5 Preferably, said first switching means comprise an insulated gate field effect MOS transistor with a gate connected to the pumped voltage and a channel connected between the pumped voltage and the electrical circuitry.

10 Preferably, said second switching means comprise an insulated gate field effect MOS transistor with a gate connected to the kicked voltage and a channel connected between the kicked voltage and the pumped voltage.

According to a further aspect of the present invention, there is provided a semiconductor memory device including:

15 a plurality of memory cells;

a plurality of word lines coupled to the memory cells;

a plurality of bit lines in pairs coupled to the memory cells;

20 a plurality of input/output lines coupled to the bit lines;

a plurality of sense amplifiers coupled to the bit line pairs, for amplifying a voltage difference between the bit lines in each pair;

25 a plurality of isolation gates coupled between the bit lines and the input/output lines; and

a plurality of word line drivers for selecting the word lines:

said semiconductor memory device further comprising:

5        a voltage pumping node coupled to electrical circuitry to which a pumped voltage is provided;

      a voltage pumping circuit for generating the pumped voltage for a power-up cycle of the semiconductor memory device;

10

      isolation means for supplying the pumped voltage to said voltage pumping node in response to the pumped voltage;

      active kicker means for compensating for a voltage drop of the pumped  
15      voltage in response to the signal output from the electrical circuitry;

      detecting means for feeding-back a sensing signal indicative of variation of the pumped voltage to said voltage pumping means; and

20        clamping means for receiving the sensing signal to clamp the pumped voltage by compensating for a voltage pull-up of the pumped voltage.

      Preferably, said voltage pumping means comprise:

25        an oscillator for generating a pumping clock in response to states of a supply voltage and the sensing signal; and

first and second charge pumps having first and second pumping nodes, said first and second charge pumps each operating complementarily in response to the pumping clock.

5            Preferably, said isolation means comprise:

         a first isolation transistor with a gate connected to the first pumping node and a channel connected between the first pumping node and the voltage pumping node; and

10

         a second isolation transistor with a gate connected to the second pumping node and a channel connected between the second pumping node and the voltage pumping node.

15            A semiconductor memory device as above may further comprise means for precharging a voltage at the first and second pumping nodes to a predetermined voltage.

20            A semiconductor memory device as above may further comprise means for precharging a voltage at the voltage pumping node to a predetermined voltage.

         Preferably, said active kicker means comprise:

25            a logic combination circuit for receiving signals from the circuitry;

         a kicking node;

a pre-kicker for setting a voltage at the kicking node to a first level when the output of the logic combination circuit is at a first state;

5 a kicking driver converting the voltage at the kicking node from said first level to a second level when the output of the logic combination circuit is at a second state; and

10 a third isolation transistor with a channel connected between the kicking node and the voltage pumping node, said third isolation transistor operating in response to the voltage at the kicking node.

Preferably, said clamping means comprise a DC current path controllable by the sensing signal, disposed in series between the pumped voltage and the supply voltage.

15

Preferably, said clamping means comprise a DC current path disposed in series between the pumped voltage and the supply voltage.

Preferably, said clamping means comprise:

20

a first clamping circuit for supplying a first voltage to the voltage pumping node if the supply voltage is identical to the first voltage; and

25

a second clamping circuit for supplying a second voltage higher than the first voltage to the voltage pumping node if the supply voltage is identical to the second voltage.

The invention extends to a semiconductor memory device provided with a voltage pumping circuit according to any of the preceding aspects of the invention.

5 For a better understanding of the invention, and to show how the same may be carried into effect, reference will now be made, by way of example, to the accompanying diagrammatic drawings, in which:

10 Figure 2 is a block diagram illustrating an embodiment of a voltage pumping circuit according to the present invention;

Figure 3A is a circuit diagram showing a specific embodiment of the circuit of Figure 2;

15 Figure 3B is a timing diagram showing an example of operation of the circuit as shown in Figure 3A;

Figure 3C is a circuit showing another specific embodiment of the circuit Figure 2;

20

Figure 4 is a block diagram illustrating a second embodiment of a voltage pumping circuit according to the present invention;

25 Figure 5A is a circuit showing a specific embodiment of the circuit of Figure 4;

Figure 5B is a timing diagram showing an example of operation of the circuit as shown in Figure 5A;



Figure 5C is a circuit showing another specific embodiment of the circuit Figure 4;

5      Figure 5D is a circuit showing a further specific embodiment of the circuit of Figure 4;

Figure 6 is a block diagram illustrating a third embodiment of a voltage pumping circuit according to the present invention;

10      Figure 7A is a circuit showing a structural embodiment of the pumping circuit of Figure 6;

Figure 7B is a circuit showing a specific embodiment of the pumping circuit of Figure 7A;

15

Figure 7C is a circuit showing a specific embodiment of an active kicker of the circuit of Figure 6;

20      Figure 7D is a timing diagram illustrating an example of operation of the active kicker of Figure 7C;

Figure 7E is a circuit showing an embodiment of a detector of Figure 6;

25      Figure 7F to 7H are circuits showing an embodiment of a clamper of Figure 6; and

Figure 8 is a timing diagram illustrating an example of operation of the circuit of Figure 6.

5 There will now be described three examples for applying principles according to the present invention, but it will be readily appreciated by those skilled in the art that further examples or embodiments of the present invention may be obtained without departing from the gist of the present invention.

10

### EXAMPLE 1

Referring to Figure 2, an oscillator control clock signal is generated simultaneously with powering a chip in order to drive an oscillator 100 when a detector (not shown) detects that voltage  $V_{pp}$  is not at a given level. The  
15 oscillator 100 generates a pulse signal whose voltage is amplified through a driver circuit 200. The amplified pulse signal is transferred to a voltage pumping circuit 300 to produce a given raised voltage  $V_{pp}$ . A bias circuit 400 precharges the output terminal of the voltage pumping circuit 300 with the level of a source voltage  $V_{cc}$  simultaneously with powering the chip. The  
20 driver circuit 200 is to improve the efficiency of the generation and voltage raising of the voltage  $V_{pp}$ .

A preferred embodiment of the circuit of Figure 2 is shown in Figure 3A. Input circuit 1115 comprises a NOR-gate 13 and NAND-gate 14. The  
25 output signal of the input circuit is voltage-amplified through a driver circuit 2128. The output signals of the driver circuit are connected to the capacitors C1, C2, C3, C4 of a voltage raising circuit. The capacitors C2 and C3 are respectively connected to the channels of first and second transfer transistors

M1 and M2. The electrodes of the capacitors C2 and C3 facing towards the channels of the transfer transistors M1 and M2 are supplied with the source voltage  $V_{cc}$  from a first bias circuit 3134. The gates of the first and second transfer transistors M1 and M2 are supplied with the source voltage  $V_{cc}$  from  
5 a second bias circuit 3538.

The operation of the circuit of Figure 3A is now specifically described with reference to Figure 3B. It should be noted that the voltage  $V_{pp}$  is continuously pumped regardless of the output phase of the oscillator being  
10 "high" or "low". In addition, the inverters 25, 26 and capacitor C1 disposed between the output terminal of the NOR-gate 13 and the gate of the first transfer transistor M1, the inverters 27, 28 and capacitor C4 between the inverter 15 connected to the output terminal of the NAND-gate 14 and the gate of the second transfer transistor M2, and the second bias circuit 3538 are  
15 to maximize the efficiency of the voltage pumping circuit. When the chip is powered up, the nodes N1 and N2 are initialized or precharged with the source voltage level ( $V_{cc}$ : precisely speaking, this will be  $V_{cc}-V_{th}$  level, but may be accomplished at  $V_{cc}$  level by replacing the components of the first bias circuit 3134 with P-type MOS transistors). If the oscillator works as  
20 shown in Figure 3B, the nodes N1 and N2 have opposite phases triggered from  $V_{cc}$  level to  $2V_{cc}$  level (this is accomplished by the coupling effect of the capacitors C2 and C3). The nodes N3 and N4 are also triggered from  $V_{cc}$  level to  $2V_{cc}$  level by the coupling effect of the capacitors C1 and C4. Accordingly the voltage  $V_{pp}$  is gradually raised from the initial  $V_{cc}$  level to  
25  $2V_{cc}$  level by the charge sharing through the first and second transfer transistors M1 and M2, as shown in Figure 3B. In this case, since the NOR-gate 13 and inverter 15 have opposite output phases, the turning-on operations of the first and second transfer transistors M1 and M2 are oppositely

performed, continuously pumping the voltage  $V_{pp}$  to  $2V_{cc}$  level. In addition, since the gates of the first and second transfer transistors M1 and M2 are continuously supplied with the voltage  $V_{cc}$  by the second bias circuit 3538, the channels of the first and second transfer transistors M1 and M2 are fully  
5 turned on when the node N1 or N2 is at  $2V_{cc}$  level, thus further improving the pumping efficiency of the voltage  $V_{pp}$ . Further the voltage  $V_{pp}$  is generated at a given level, i.e.  $2V_{cc}$  before enabling of the chip, thereby achieving high speed operation of the chip. In the case of the circuit as shown in Figure 3A, a high raised voltage is obtained even at a considerably  
10 low operating source voltage  $V_{cc}$  of the chip, so that the  $V_{pp}$  voltage has a value of 4.5V or more with a  $V_{cc}$  voltage of 3V.

The circuit of Figure 3C is similar to the circuit of Figure 3A except that the first and second transfer transistors M10 and M20 are diode-  
15 connected. Comparing Figure 3C with Figure 3A, there are eliminated the inverters 25, 26 and capacitor C1 connected to the gate of the first transfer transistor M1, the inverters 27, 28 and capacitor C4 connected to the gate of the second transfer transistor M2, and the second bias circuit 3538. The operational characteristics of Figure 3C are similar to Figure 3A. The voltage  
20 of the node N10 or N20 is raised to  $2V_{cc}$  level to turn on the first or second transfer transistor M10 or M20, thus raising the  $V_{pp}$  voltage to a given level. The circuit of Figure 3C is so simple as to be suitably used in a chip of high complexity. The technical concept as shown in Figure 2 may be realized in a variety of embodiments in addition to the circuits of Figures 3A and 3C.  
25 For example, the input circuit may take any form provided it should make logically different responses to the output waveform of the oscillator, and the first and second bias circuits may also take any form provided they supply  $V_{cc}$  (or  $V_{cc}-V_{th}$ ) voltage.

## EXAMPLE 2

Referring to Figure 4, an enable signal is applied to a source voltage precharge circuit 50 and the control circuit 70 of an output circuit M. The Vpp signal is transferred from the channel of the output circuit M to the output terminal of the voltage pumping circuit (i.e. Vpp voltage generator) provided on a chip. The source voltage precharge circuit 50, which is to improve the efficiency of the voltage pumping circuit 60, causes the voltage pumping circuit 60 to pump the output voltage to a given level, and initially precharges the voltage pumping circuit 60 with the source voltage Vcc when the circuit of Figure 4 is disabled. The control circuit 70 controls the output circuit M to perform an output operation only when the raised voltage Vpp applied to the chip is dropped. The output circuit also serves to prevent the raised voltage Vpp (i.e. the voltage generated by the voltage pumping circuit provided in the chip) from flowing in reverse into the voltage pumping circuit when the circuit of Figure 4 is disabled. In this example, the output circuit M consists of an N-type MOS transistor, but may take any other form to transfer the raised voltage Vpp.

There are shown specific embodiments of the circuit of Figure 4 in Figures 5A, 5C and 5D. The circuits of Figures 5A, 5C and 5D have different input circuits according to the kind of the enable signal or the operational mode of the chip. Namely, the active operation of the chip has a variety of modes such as data read/write, chip test, etc., and accordingly the enable signal is set variously. Hence, the circuits of Figures 5A, 5C and 5D are to compensate for the voltage drop occurring in each active operation.

The circuit of Figure 5A comprises an input circuit 10A for supplying an enable signal, source voltage precharge circuit 50 connected to receive the output signal of the input circuit 10A, voltage pumping circuit 60 connected to receive the output signal of the input circuit 10A for raising the output signal voltage of the source voltage precharge circuit 60, output circuit M7 for transferring the raised voltage of the voltage pumping circuit 60, and output control circuit 70 for controlling the operation of the output circuit M7. The inverters 61, 62,...,66 are suitably used for effective connection of the circuit elements. The input circuit 10A consists of a NAND-gate 71 with two inputs respectively receiving two enable signals PTRST and PRD, NOR-gate 74 with one input receiving the enable signal PRD via an inverter 73 and other input receiving the output signal of the NAND-gate 71 via an inverter 72, and inverter 75 connected to the output of the NOR-gate 74.

The source voltage precharge circuit 60 comprises a first voltage pumping capacitor C1, first pull-up transistor M1, second pull-up transistor M2, third pull-up transistor M4 and fourth pull-up transistor M3. One electrode of the capacitor C1 is connected to receive the output signal of the input circuit 10A via inverters 61, 62, 63. The first pull-up transistor M1 has a gate connected with the source voltage Vcc and a channel between the source voltage and the other electrode of the first capacitor C1. The second pull-up transistor M2 has a gate connected with an output node N6 and a channel between the source voltage and the other electrode of the first capacitor C1. The third pull-up transistor M4 has a gate connected with the voltage source Vcc and a channel between the voltage source and output node N6. The fourth pull-up transistor M3 has a gate connected with the other electrode of the first capacitor C1 and a channel between the voltage source and output node N6.

The voltage pumping circuit 60 consists of a second voltage pumping capacitor C2 with one input connected to receive the output signal of the input circuit 10A via inverters 64, 65 and driver circuit 77, 78 for improving the voltage pumping efficiency. The output control circuit 60 consists of a third pumping capacitor C3 with one electrode connected to receive the output signal of the input circuit 10A via inverters 64, 65, fourth pumping capacitor C4 with one electrode connected to receive the output signal of the input circuit 10A via an inverter 66, fifth pull-up transistor M5 with a gate connected to the source voltage Vcc and a channel between the source voltage and the other electrode of the fourth capacitor C4, and sixth pull-up transistor M6 with a gate connected to the other electrode of the fourth capacitor C4. A channel of the sixth pull-up transistor M6 has one end connected with the source voltage and the other end connected commonly with the other electrode of the third capacitor C3 and the control terminal of the output circuit M7. The output node N6 of the voltage pumping circuit 60 transfers the raised voltage Vpp and is fed back to the control terminal of the second pull-up transistor M2. The enable signals PTRST and PRD perform transition respectively when the column and row address signals are produced as active signals.

The operational characteristics of the circuit of Figure 5A are described with reference to the timing diagram of Figure 5B. The enable signals PTRST and PRD are produced in "low" state as shown in Figure 5B when they do not perform a transition (or the chip is not in active operation). The timing diagram of Figure 5B represents the operations after the circuit of Figure 5A is activated. When the circuit of Figure 5A is disabled, the nodes N6 and N4 are all precharged with the source voltage Vcc. The node N1 for receiving the output signal of the input circuit 10A is precharged with ground

voltage, the node N5 of the source voltage precharge circuit 50 with  $2V_{cc}$ , and the output node N6 of the voltage pumping circuit 60 with the source voltage. The node N4 is precharged with  $V_{cc}$  connected to the control terminal of the output circuit M7 which is disabled. Thereafter the chip is  
5 activated, while the node N5 of the source voltage precharge circuit 50 is precharged with the source voltage and the output node N6 of the voltage pumping circuit 60 with  $2V_{cc}$ . The node N3 of the output control circuit 60 is precharged with  $V_{cc}$  and the node N4 with  $2V_{cc}$  applied to the control terminal of the output circuit M7. When the enable signal PRD is firstly  
10 raised to "high" level (the enable signal PRD is produced delayed after a row address strobe signal (RAS) is produced as an active signal), the voltage level of the node N1 is changed to "low", and accordingly the node N5 to  $2V_{cc}$  and the nodes N6 and N4 to  $V_{cc}$ .

15 In this case, the node N6 is at full- $V_{cc}$  voltage level supplied through the third pull-up transistor M3 which is fully turned on by the node N5 at  $2V_{cc}$  voltage level, so that it is pumped fully to  $2V_{cc}$  level when the node N1 performs transition to "high" level. Meanwhile, the output circuit M7 is turned off, which indicates that the chip is activated to apply the  $V_{pp}$  voltage  
20 to the components of the chip (i.e. components such as word line driver, data output driver, etc.). Then if the enable signal PTRST transits to "high" level (in this case, the enable signal PRD keeps "high" level), the node N1 takes "high" level causing the nodes N5, N6, N4 respectively to have  $V_{cc}$ ,  $2V_{cc}$  and  $2V_{cc}$ . The  $V_{pp}$  voltage is used as the operating voltage of the chip, thus  
25 suffering a voltage drop. At this time, the output circuit M7, whose control terminal is applied with  $2V_{cc}$  and channel is charged with  $2V_{cc}$  at one end, is turned on to quickly compensate for the voltage drop of the  $V_{pp}$  voltage. Thus the components of the chip using  $V_{pp}$  as the operating voltage keep



stable operations, and the operational speed is not slowed down. Then if the enable signal PTRST becomes "low", the node N1 again takes "low" level, causing the node N5 to have  $2V_{cc}$  level and the nodes N6 and N4 to have  $V_{cc}$  level, so that the  $V_{pp}$  voltage is prevented from flowing in reverse through the output circuit M7. Further, if the enable signal PRD becomes low, each component is precharged with the initial value and thereafter the dropping of the  $V_{pp}$  voltage is properly compensated. In Figure 5B, the interval Q in which the  $V_{pp}$  voltage is substantially compensated may be properly adjusted according to the characteristics of the chip by controlling the time of the enabling signal or providing the voltage pumping circuit with a delay circuit.

The circuit of Figure 5C is similar to that of Figure 5A except for the enable signals input to the input circuit 10B and the construction of the logic gate thereof. The enable signal PXIE is to control the raised voltage  $V_{pp}$  of the voltage pumping circuit to be applied to a given word line, and the enable signal PDPX is produced when the RAS performs transition or a given address is decoded performing transition. The input circuit 10B consists of a first NAND-gate 81 and NOR-gate 82 each with two inputs respectively receiving the two enable signals PXIE and PDPX and a second NAND-gate 84 for receiving the output of the NOR-gate 82 via an inverter 83. The node N1 for receiving the output signal of the input circuit 10B is precharged with "high" level as in the case of Figure 5A, and the other circuits also work as in the circuit of Figure 5A. The enable signals PXIE and PDPX are clock signals widely applied to a variety of the operational modes of a dynamic RAM.

The circuit of Figure 5D has an additional enable signal PFTE of the input circuit 10C, as compared to the circuit of Figure 5C. Hence the NAND-gate 88 for receiving the enable signal PFTE has three inputs and one output. The enable signal PFTE is enabled when a memory chip performs a test mode. The circuit of Figure 5D also works in the same manner as that of Figure 5C, and the node N1 is precharged with "high" level.

The circuits of Figures 5A, 5C and 5D have different uses according to the operational modes of the chip and therefore may all be provided on a chip. Of course, various modifications to the circuits may be made without departing the spirit of the present invention.

### EXAMPLE 3

The voltage pumping means of Figure 6 comprises a pumping circuit 500 for producing a raised voltage  $V_{pp}$ , active kicker 600 for compensating for the dropping of the raised voltage  $V_{pp}$ , detector 700 for detecting the level of the raised voltage  $V_{pp}$ , and first and second clamper 800 and 900 for preventing the raised voltage  $V_{pp}$  from being raised over a given level.

The pumping circuit 500 comprises, as shown in Figure 7A, an oscillator 110 for generating pumping clock pulses  $\Phi_{PP}$  in response to the level detection signal  $\Phi_{DET}$  of the detector 700, charge pump 130 for producing the raised voltage  $V_{pp}$  in response to the pumping clock pulses  $\Phi_{PP}$ , first precharge circuit 160 for precharging the pumping node of the output of the charge pump 130 with  $V_{cc}$  before pumping operation, isolation transistors 141, 142 for transferring the voltage of the pumping node to the

Vpp node 180, and second precharge circuit 170 for precharging the gates of the isolation transistors 141, 142 with Vcc before pumping operation.

Referring to Figure 7B for specifically illustrating the circuit of Figure 7A, the charge pump 130 comprises a first charge pump circuit 130a driven at "high" state of the pumping clock pulses  $\Phi_{PP}$  and second charge pump circuit 130b driven at "low" state of the pumping clock pulses  $\Phi_{PP}$ . The first precharge circuit 160 consists of two transmission gates 161 and 162 connected in latch configuration between the source voltage Vcc and the first and second pumping nodes 165 and 166. Likewise the second precharge circuit 170 consists of two transmission gates 171 and 172 performing latching operation to provide the gates of the isolation transistors 141 and 142 with the source voltage Vcc. The isolation transistors 141 and 142 which consist of NMOS transistors in the present embodiment transfer the voltages of the first and second pumping nodes 165 and 166 to the Vpp node 180. The first and second precharge circuits 160 and 170 work to simultaneously raise the voltages of the pumping nodes 165 and 166 and the gates of the isolation transistors 141 and 142 from the Vcc level. The pumping clock pulses  $\Phi_{PP}$  are adjusted in pulse width by means of inverters 113, 114 and changed by NAND gate 115 to first pumping clock pulses  $\Phi_{PPa}$  supplied to the first and second pumping MOS capacitors 131 and 132 of the first charge pump circuit 130a which are respectively connected with the gate and drain of the first isolation transistor 141. Further the pumping clock pulses  $\Phi_{PP}$  are adjusted in pulse width by means of the inverters 113, 114 and changed by NAND-gate 116 to second pumping clock pulses  $\Phi_{PPb}$  supplied via inverter 135 to third and fourth MOS capacitors of the second charge pump circuit 130b which are respectively connected with the drain and gate of the second isolation transistor 142. Thus, in the case of the pumping clock pulses  $\Phi_{PP}$

being low, the first and second pumping MOS capacitors 131 and 132 work to charge the  $V_{pp}$  node 180 with  $2V_{cc}$ , while in the case of the pumping clock pulses  $\Phi_{PP}$  being high the third and fourth pumping MOS capacitors 133 and 134 work to raise further the voltage level of the  $V_{pp}$  node 180 that has been already charged with  $2V_{cc}$  by means of the first charge pump circuit 130a.

The pumping circuit 500 supplies the raised voltage  $V_{pp}$  through the first and second isolation transistors 141 and 142 to the word line driver or bit line separation gate, and therefore does not require a separate capacitor as in the conventional circuit as shown in Figure 1. Moreover the raised voltage  $V_{pp}$  is supplied, already prepared, to the separation gate of a bit line, so that the N-type and P-type sense amplifiers may be commonly employed and there is no need to provide an additional circuit for raising the voltage applied to the separation gate as in the conventional circuit. This contributes to the reduction of the chip size. If the level of the source voltage  $V_{cc}$  applied to the NAND-gate to drive the oscillator is not raised over a given value (i.e. it is not in the operating state), the pumping circuit 500 does not work and therefore the operating and standby current of the chip is not substantially increased, thus reducing the power consumption needed for pumping.

The active kicker 600 is to compensate for the dropping of the raised voltage  $V_{pp}$  that is caused by the raised voltage  $V_{pp}$  of the pumping circuit 500 being repeatedly supplied to the word line driver or separation gate (the gate of the transistor for transferring data between data lines). As shown in Figure 7C, the active kicker 600 comprises an exclusive OR (XOR) circuit 210 for receiving the clock pulses  $P_{xie}$ ,  $P_{dpx}$  and source voltage  $V_{cc}$ , pre-kicker 220 operated at the output of the XOR circuit 210 being "low", and

kicking driver 230 operated at the output of the XOR circuit 210 being "high". The signals Pxie and Pdp<sub>x</sub> are used to drive selected word lines of a memory array.

5           In the pre-kicker 220, the output of the XOR circuit 210 is supplied to the first node 201 which in turn is connected with the second node 202 via three cascaded inverters 221, 222, 223 and a kicking capacitor 224. Between the second and third nodes 202 and 203 there are arranged two NMOS transistors 226 and 227 with their gates cross-coupled and their drains  
10           connected to the source voltage. The two transistors are to precharge the third node 203 with full V<sub>cc</sub> by employing the voltage of the second node 202. Between the first and third nodes 201 and 203 there are connected in series four inverters 231, 232, 233, 234 and second kicking capacitor 235. The first node 201 is connected with the fourth node 204 via inverter 239 and  
15           third kicking capacitor 241. The fourth node 204 is charged with V<sub>cc</sub>-V<sub>th</sub> level by means of the NMOS transistor 238 connected to the source voltage V<sub>cc</sub>. Also the fourth node 204 is connected with the gate of a precharge NMOS transistor 237 with the drain connected to the source voltage. The source of the NMOS transistor 237 is connected with the fifth node 205.  
20           Between the inverter 232 and fifth node 205 is connected fourth kicking capacitor 236. The V<sub>pp</sub> node 180 is connected with the source of the third isolation transistor 240 whose gate and drain are respectively connected to the fifth and third nodes 205 and 203.

25           Referring to Figure 7D based on Figure 7C, when the first node 201 connected with the output of the XOR circuit 210 is in "low" state, the three inverters 221, 222, 223 and first kicking capacitor 224 connected in series with the first node 201 work to raise voltage level of the second node 202

from  $V_{cc}-V_{th}$  (precharged by means of the NMOS transistor 225) to  $2V_{cc}-V_{th}$ . This causes the NMOS transistors 226 and 227 to charge the third node 203 with full  $V_{cc}$  level. Since the voltage level of the fourth node 204 is raised from  $V_{cc}-V_{th}$  to  $2V_{cc}-V_{th}$  during the first node 201 being in "low" state, the fifth node 205 is charged with full  $V_{cc}$  level via the NMOS transistor 237. Thereafter, when the voltage level of the first node 201 becomes "high", the voltage level of the third node 203 is raised from  $V_{cc}$  level to  $2V_{cc}$  level by the operation of the fourth kicking capacitor 236. Likewise the fourth kicking capacitor 236 works to raise the voltage level of the fifth node 205 from  $V_{cc}$  level to  $2V_{cc}$  level. Thus the isolation transistor 240 supplies  $2V_{cc}$  to the  $V_{pp}$  node 180. In this active kicker 200, the source voltage  $V_{cc}$  is one input to the XOR circuit 210 and therefore will not drive the circuit below a given level as in the pumping circuit 500. In addition, since the signals  $P_{xie}$  and  $P_{dpx}$  are produced from the circuit using the raised voltage  $V_{pp}$  (e.g. the word line driver), the dropping of the raised voltage  $V_{pp}$  may be compensated by means of the above procedure. The number of the active kickers is proportional to that of the circuits using the raised voltage  $V_{pp}$ .

Referring to Figure 7E, the raised voltage  $V_{pp}$  is applied to the gate of NMOS transistor 310 and its level is detected. Hence, the threshold voltage of the NMOS transistor 310 connected between the source voltage and detection node 301 should be set to the value that turns on or off the transistor according to the gate voltage being over or below  $2V_{cc}$ , assuming the raised voltage  $V_{pp}$  is  $2V_{cc}$ . Methods for setting the threshold voltage of the NMOS transistor are well-known in this art and therefore not described. Between the detection node 301 and ground voltage  $V_{ss}$  is arranged an NMOS transistor 320 with a gate connected to a reference voltage  $V_{ref}$ . Assuming that a

constant resistance between the detection node 301 and ground voltage  $V_{ss}$  is  $R_{ref}$ , and that between the source voltage and detection node 301  $R_{pp}$  (varied according to the level of the raised voltage  $V_{pp}$ ), the voltage of the detection node 301 is determined by the ratio  $R_{ref}/(R_{pp}+R_{ref})$ . Hence, if the level of the raised voltage  $V_{pp}$  becomes low, the value of  $R_{pp}$  increases, lowering the voltage of the detection node. Then, through the three inverters 340, 350, 360 and 370, 380, 390 are generated the detection signal  $\Phi_{DET}$  and clamp signal  $\Phi_{CLMP}$  with high state. On the contrary, if the level of the raised voltage  $V_{pp}$  becomes high, the reduced  $R_{pp}$  causes an increase of the voltage of the detection node 301 and therefore the detection signal  $\Phi_{DET}$  and clamp signal  $\Phi_{CLMP}$  become low. As shown in Figure 7A, the detection signal  $\Phi_{DET}$  of high state is fed back to the pumping circuit 500 to drive the oscillator 110 to perform the  $V_{pp}$  pumping operation, thus raising the reduced level of the raised voltage  $V_{pp}$ . If the detection signal  $\Phi_{DET}$  is in a low state, the oscillator 110 is disabled, no longer performing the pumping operation.

Referring to Figure 7F, there are shown first and second clampers 800 and 900 for preventing the voltage  $V_{pp}$  from being raised to an undesirable level. These serve to pull the excessively raised voltage  $V_{pp}$  down to the source voltage  $V_{cc}$  in order to prevent destruction of the components when the level of the raised voltage  $V_{pp}$  exceeds a given value. Namely, as shown in Figure 7F, when the level of the raised voltage  $V_{pp}$  increases, the detector 700 produces a clamp signal  $\Phi_{CLMP}$  of low state applied to the gate of the PMOS transistor 410, so that the excessively raised voltage  $V_{pp}$  is discharged via the channels of the cascaded NMOS transistors 420, 430 and PMOS transistor 410 to the source voltage terminal. In this case, the raised voltage  $V_{pp}$  is dropped through the NMOS transistor 430 by about  $V_{cc}+V_{th}$ . The

circuit of Figure 7G uses the cascaded NMOS transistors 510, 520 and PMOS transistor 530 to discharge the raised voltage  $V_{pp}$  without using the signal  $\Phi_{CLMP}$  as in Figure 7F. Of course, the raised voltage  $V_{pp}$  is dropped through the NMOS transistor 520 by  $V_{cc} + V_{th}$ . The pull-down level of the raised voltage is determined by the number ( $n$ ) of the NMOS transistors cascaded between the  $V_{pp}$  terminal and  $V_{cc}$  terminal to contribute to the voltage dropping. The circuits of Figures 7F and 7G show the case of  $n=1$ . If there are used  $n$  cascaded NMOS transistors to contribute to the voltage dropping, the raised voltage  $V_{pp}$  will be dropped by  $V_{cc} + V_{th}$ .

In Figure 7H, the clamper 800 includes two clamper circuits arranged between the  $V_{cc}$  and  $V_{pp}$  terminals. The clamper circuit 1 has the same structure as the circuit of Figure 7F and the clamper circuit 2 is similar to the circuit of Figure 7G while eliminating the PMOS transistor 530 whose gate is grounded in Figure 7G. Assuming that the threshold voltages of the NMOS transistors 420, 520, 510 are respectively  $V_{th1}$ ,  $V_{th2}$ ,  $V_{th3}$  (in this case, the relationship between the threshold voltages is assumed  $V_{th1} < V_{th2} + V_{th3}$ ), the clamper circuit 1 works in the same manner as the circuit of Figure 7F. In the clamper circuit 2, if the voltage level of the node C has the value of  $V_{cc} + V_{th2}$ , the NMOS transistor 520 is turned on, and if the voltage level of the  $V_{pp}$  terminal has the value of  $V_{cc} + V_{th2} + V_{th3}$  or more, the NMOS transistor 510 is turned on, so that a current path is formed between the  $V_{cc}$  and  $V_{pp}$  terminals to discharge the voltage. Thus, in Figure 7H, until the voltage level of the  $V_{cc}$  terminal comes to be within the range of  $V_{cc} + V_{th2}$  to  $V_{cc} + V_{th2} + V_{th3}$ , the clamper circuit 1 uses the clamp signal  $\Phi_{CLMP}$  to adjust the voltage level of the  $V_{pp}$  terminal as desired, and the voltage level of the  $V_{pp}$  terminal exceeding the value of  $V_{cc} + V_{th2} + V_{th3}$ , the clamper circuit 2 turns on the NMOS transistors 520 and 510 to discharge the voltage



to the  $V_{pp}$  terminal. Hence, the voltage level of the  $V_{pp}$  terminal may be adjusted to have any value between  $V_{cc}+V_{th2}+V_{th3}$  and  $V_{cc}+V_{th1}$ .

Hereinafter, the operation of the above circuit is described with  
5 reference to Figure 8, where arrow lines show the relationship between signals.

Before supplying the source voltage  $V_{cc}$  (low state), the output of the inverter 112 of the pumping circuit 500 is low and therefore the pumping  
10 clock pulses  $\Phi_{PP}$  are kept "high". Supplying the source voltage, the first and second pumping nodes 165 and 166 and the gates of the first and second isolation transistors 141 and 142 are precharged with the source voltage  $V_{cc}$  by means of the first and second precharge circuits 160 170. This in turn precharges the  $V_{pp}$  node 180 with  $V_{cc}-V_{th}$ . The oscillator periodically  
15 produces the pumping clock pulses  $\Phi_{PP}$ . Then the first and second pumping clock pulses  $\Phi_{PPa}$  and  $\Phi_{PPb}$  that complementarily work in response to the pumping clock pulses  $\Phi_{PP}$  cause the first and second pumping nodes 165 and 166 and the gates of the first and second isolation transistors 141 and 142 to have the voltage level of  $2V_{cc}$ . Consequently the voltage of the  $V_{pp}$  node  
20 180 is raised to  $2V_{cc}$ . This raised voltage  $V_{pp}$  of  $2V_{cc}$  is dropped due to charge sharing when supplied to the word lines, separation gates, etc. (see 801 and 802 in Figure 8). In order to compensate for this voltage dropping, there is used the active kicker 200 of Figure 5, whose operation has been described with reference to Figure 5B. Meanwhile, if the raised voltage  $V_{pp}$   
25 is excessively raised owing to excessive pumping, the clamp signal  $\Phi_{CLMP}$  becomes low in Figure 7E. This causes the level of the raised voltage  $V_{pp}$  to be dropped by  $V_{cc}+V_{th}$  (see 803 in Figure 8). When the clamp signal  $\Phi_{CLMP}$  is low, the detection signal  $\Phi_{DET}$  is also low. This causes the

pumping clock pulses  $\Phi_{PP}$  to be kept high as in the initial disabled state. Thus the pumping circuit 500 no longer performs the pumping operation, so that the level of the raised voltage  $V_{pp}$  may be excessively dropped (see 804 in Figure 8). However, in this case, the detection signal  $\Phi_{DET}$  is made high  
5 to restart the pumping operation.

As described above, the active kicker 600 compensates for the dropping of the raised voltage  $V_{pp}$ , the detector 700 keeps the present  $V_{pp}$  level stable, and the clampers 800 and 900 prevent the raised voltage  $V_{pp}$  from being  
10 excessively raised. Furthermore, the pumping circuit 500 of Figure 7B and the active kicker 600 of Figure 7C are used to supply the raised voltage to the bit line isolation transistors without using capacitors as in the conventional circuit of Figure 1C, so that the N-channel and P-channel sense amplifiers may be commonly used, thus reducing the chip size. In addition, the  
15 pumping circuit 500 works only with receiving the source voltage  $V_{cc}$ , thereby reducing the power consumption of the chip.

Various modifications and embodiments of the circuits described above with reference to the attached drawings may be obtained without departing  
20 from the scope of the inventive concept.

Thus, embodiments of the present invention may provide a voltage pumping circuit used in a semiconductor memory device of high complexity, whereby the source voltage may be raised and maintained to be suitably  
25 adapted to the components of the device.

The reader's attention is directed to all papers and documents which are filed concurrently with or previous to this specification in connection with this

application and which are open to public inspection with this specification, and the contents of all such papers and documents are incorporated herein by reference.

5 All of the features disclosed in this specification (including any accompanying claims, abstract and drawings), and/or all of the steps of any method or process so disclosed, may be combined in any combination, except combinations where at least some of such features and/or steps are mutually exclusive.

10

Each feature disclosed in this specification (including any accompanying claims, abstract and drawings), may be replaced by alternative features serving the same, equivalent or similar purpose, unless expressly stated otherwise. Thus, unless expressly stated otherwise, each feature  
15 disclosed is one example only of a generic series of equivalent or similar features.

The invention is not restricted to the details of the foregoing embodiment(s). The invention extends to any novel one, or any novel  
20 combination, of the features disclosed in this specification (including any accompanying claims, abstract and drawings), or to any novel one, or any novel combination, of the steps of any method or process so disclosed.

CLAIMS

1. A semiconductor memory device arranged to be powered by a supply voltage, and comprising an oscillator for generating pulses, and a voltage  
5 pumping circuit for generating at an initial power-up state a first output voltage which is substantially identical to said supply voltage, and pumping an output voltage up to a second output voltage prior to or upon the semiconductor memory device being enabled in response to pulses output from said oscillator, said second output voltage being higher than said first  
10 output voltage.

2. A semiconductor memory device as claimed in claim 1, further comprising a detector for detecting variation of the output of said voltage pumping circuit, whereby said voltage pumping circuit operates to control the  
15 pumping operation thereof in response to the detection so as to maintain the output at said second output voltage.

3. A semiconductor memory device as claimed in claim 1 or 2, wherein said voltage pumping circuit comprises:

20 input means operating in response to the pulses output from said oscillator;

voltage pumping means for generating said second output voltage in  
25 response to the output of said input means; and

bias means for forcing at the initial power-up state the output of said voltage pumping circuit into said first output voltage.

4. A semiconductor memory device as claimed in claim 3, wherein said input means receive the pulses output from said oscillator to generate a pair of complementary signals.

5. A semiconductor memory device as claimed in claim 3 or 4, further comprising driving means for amplifying the output signals of said input means.

6. A semiconductor memory device as claimed in claim 5, wherein said voltage pumping means comprise a plurality of capacitors each having first and second electrodes, said first electrodes being respectively coupled to the output signals of said driving means.

7. A semiconductor memory device as claimed in any of the preceding claims, further comprising first and second transmission transistors for providing said second output voltage to an output terminal by means of a charge sharing occurring through channels thereof, gates and selected first terminals of the channels of said first and second transmission transistors being respectively coupled to the second electrodes of said capacitors.

8. A semiconductor memory device as claimed in claims 4 and 7, wherein said first and second transmission transistors are alternatively turned-on and turned-off in response to the complementary signals output from said input means.

9. A semiconductor memory device as claimed in claim 8 or claims 3 and 7, wherein said bias means comprise:

a first bias circuit for providing the supply voltage to said first terminals of the channels of said first and second transmission transistors; and

5 a second bias circuit for providing the supply voltage to the gates of said first and second transmission transistors.

10. A semiconductor memory device as claimed in claim 9, wherein said first and second bias circuits in association with each other provide the output terminal with said first output voltage at the initial power-up state.

10

11. A voltage pumping circuit being provided with a supply voltage, and an oscillator for generating pulses, and comprising:

15 input means operating in response to pulses generated by said oscillator;

voltage pumping means for pumping up the output of said input means to generate a pumped voltage in response to the output of said input means; and

20

bias means for providing an output terminal of said voltage pumping means with the supply voltage.

25 12. A voltage pumping circuit as claimed in claim 11, further comprising a detector for detecting variation of the output voltage of said voltage pumping circuit, whereby said voltage pumping circuit operates to control the pumping operation thereof in response to the detection so as to maintain the output voltage at said pumped voltage.

13. A voltage pumping circuit as claimed in claim 11 or 12, wherein said input means receive the pulses output from said oscillator to generate a pair of complementary signals.

5 14. A voltage pumping circuit as claimed in claim 11, 12 or 13, wherein said voltage pumping means comprise a plurality of capacitors each having first and second electrodes, said first electrodes being respectively coupled to the output signals of said input means.

10 15. A voltage pumping circuit as claimed in claim 14, further comprising first and second diode-connected transmission transistors for providing the output voltage of said voltage pumping means to an output terminal by means of a charge sharing occurring through channels thereof, gates and selected first terminals of the channels of said first and second transmission transistors  
15 being respectively coupled to the second electrodes of said capacitors.

16. A voltage pumping circuit as claimed in claim 13 and 15, wherein said first and second diode-connected transmission transistors are alternatively turned-on and turned-off in response to the complementary signals output from  
20 said input means.

17. Voltage pumping circuit as claimed in claim 15 or 16, wherein said bias means provide the first terminal of the channel of said first and second diode-connected transmission transistors with the supply voltage.

25

18. A voltage pumping circuit in a semiconductor memory device having an oscillator for generating pulses, the circuit comprising:

input means operating in response to pulses output from said oscillator;

driver means for amplifying the output signals of said input means;

5        voltage pumping means comprising a plurality of capacitors each having first and second electrodes, said first electrodes being respectively coupled to the output signals of said driver means;

10        bias means for forcing at an initial power-up state the output voltage of said voltage pumping means to the supply voltage level; and

transmission means coupled to the output of said voltage pumping means, for generating a pumped voltage.

15        19. A voltage pumping circuit as claimed in claim 18, wherein said input means receive the pulses output from said oscillator to generate a pair of complementary signals.

20        20. A voltage pumping circuit as claimed in claim 18 or 19, further comprising a detector for detecting variation of the output of said voltage pumping circuit, whereby said voltage pumping circuit operates to control the pumping operation thereof in response to the detection so as to maintain the output voltage at said pumped voltage.

25        21. A voltage pumping circuit for a semiconductor memory device, the circuit having a voltage pumping node to which a pumped voltage higher than a supply voltage is applied, and comprising:



input means for receiving an enable signal input;

voltage pumping means for generating said pumped voltage in response to the output of said input means; and

5

output means for supplying the pumped voltage of said voltage pumping means;

10 whereby if said pumped voltage decreases during an active operation mode of the semiconductor memory device such as an enable mode or a test mode of the semiconductor memory device, said pumped voltage is compensated by the lowered voltage.

15 22. A voltage pumping circuit as claimed in claim 21, further comprising precharge means for precharging the output of said voltage pumping means to the supply voltage during disable of the voltage pumping circuit, so as to increase voltage pumping efficiency of said voltage pumping means.

20 23. A voltage pumping circuit as claimed in claim 21 or 22, wherein said voltage pumping circuit is enabled only for the active operation mode of the semiconductor memory device.

25 24. A voltage pumping circuit as claimed in claim 21, 22 or 23, wherein said voltage pumping means comprise at least one voltage pumping capacitor responsive to the output of said input means.

25. A voltage pumping circuit as claimed in claim 22 or claim 23 or 24 as appendant thereto, wherein said precharge means comprise:

at least one voltage pumping capacitor responsive to the output of said input means; and

5 a plurality of pull-up transistors coupled between the voltage pumping capacitor and the pumped voltage output;

whereby an initial output voltage of said voltage pumping means is precharged to the supply voltage through the pull-up transistors during a non-active operation mode of the semiconductor memory device.

10

26. A voltage pumping circuit as claimed in any of claims 21 to 25, wherein said enable signal is a signal generated in association with row or column address strobe signals, or a signal generated upon a power-up of the semiconductor memory device.

15

27. A voltage pumping circuit for a semiconductor memory device, the circuit having a voltage pumping node to which a pumped voltage higher than a supply voltage is applied, and comprising:

20 input means for receiving an enable signal input;

voltage pumping means for generating said pumped voltage in response to the output of said input means;

25 precharge means coupled to the output of said input means, for precharging the output of said voltage pumping means to the supply voltage during a non-active operation mode of the semiconductor memory device;

output means for supplying the pumped voltage of said voltage pumping means during an active operation mode of the semiconductor memory device; and

5            output control means for controlling operation of said output means in response to the output of said input means.

28.    A voltage pumping circuit as claimed in claim 27, wherein said voltage pumping means comprise:

10

a driver circuit coupled to the output of said input means; and

a first voltage pumping capacitor having first and second electrodes, the first electrode being coupled to the output of said driver circuit.

15

29.    The voltage pumping circuit as claimed in claim 27 or 28, wherein said precharge means comprise:

20

a second voltage pumping capacitor having first and second electrodes, the first electrode being coupled to the output of said input means;

a first pull-up transistor with a gate connected to the supply voltage and a channel connected between the supply voltage and the second electrode of said second voltage pumping capacitor;

25

a second pull-up transistor with a gate connected to the output of said voltage pumping means and a channel connected between the supply voltage and the second electrode of said second voltage pumping capacitor;

a third pull-up transistor with a gate connected to the supply voltage and a channel connected between the supply voltage and the output of said voltage pumping means; and

5           a fourth pull-up transistor with a gate connected to the second electrode of said second voltage pumping capacitor and a channel connected between the supply voltage and the output of said voltage pumping means.

30.    A voltage pumping circuit as claimed in claim 27, 28 or 29, wherein  
10   said output control means comprise:

          a third voltage pumping capacitor having first and second electrodes, the first electrode being connected to the output of said input means, and the second electrode being connected to a control terminal of said output means;  
15

          a fourth voltage pumping capacitor having first and second electrodes, the first electrode being connected to the output of said input means;

          a fifth pull-up transistor with a gate connected to the supply voltage and  
20   a channel connected between the supply voltage and the second electrode of said fourth voltage pumping capacitor; and

          a sixth pull-up transistor with a gate connected to the second electrode of said fourth voltage pumping capacitor and a channel connected between the  
25   second electrode of said third voltage pumping capacitor and the supply voltage.

31. A voltage pumping circuit as claimed in any of claims 27 to 30, wherein said enable signal is a signal generated in association with row or column address strobe signals, or a signal generated upon power-up of the semiconductor memory device.

5

32. A voltage pumping circuit for a semiconductor memory device, the circuit comprising:

10 an input node for sensing transition of an enable signal input, for compensating for a voltage drop of a pumped voltage output from the voltage pumping circuit, comprising:

voltage pumping means for generating said pumped voltage in response to transition of the enable signal input at said input node;

15

precharge means coupled to said input node, for precharging the output of said voltage pumping means to a supply voltage during a non-active operation mode of the semiconductor memory device;

20

output means for supplying the pumped voltage of said voltage pumping means during an active operation mode of the semiconductor memory device; and

25

output control means for controlling operation of said output means in response to the enable signal input at the input node.

33. A voltage pumping circuit as claimed in claim 32, wherein said enable signal is a signal generated in association with row or column address strobe

signals, or a signal generated upon a power-up of the semiconductor memory device.

34. A semiconductor memory device having electrical circuitry provided  
5 with a pumped voltage higher than a supply voltage, the device comprising:

- a voltage pumping node coupled to the circuitry;

10 voltage pumping means for pumping up a voltage for a power-up cycle of the semiconductor memory device, to generate the pumped voltage;

isolation means for supplying the pumped voltage to said voltage pumping node in response to the pumped voltage;

15 active kicker means for compensating for a voltage drop of the pumped voltage in response to the signal output from the circuitry;

20 detecting means for feeding-back a sensing signal indicative of variation of the pumped voltage to said voltage pumping means; and

clamping means for receiving the sensing signal to clamp the pumped voltage to compensate for a voltage pull-up of the pumped voltage.

35. A semiconductor memory device as claimed in claim 34, wherein said  
25 voltage pumping means comprise:

an oscillator for generating a pumping clock in response to states of the supply voltage and the sensing signal; and

first and second charge pumps having first and second pumping nodes, said first and second charge pumps each operating complementarily in response to the pumping clock.

- 5     36.     A semiconductor memory device as claimed in claim 35, wherein said isolation means comprise:

10           a first isolation transistor with a gate connected to the first pumping node and a channel connected between the first pumping node and the voltage pumping node; and

15           a second isolation transistor with a gate connected to the second pumping node and a channel connected between the second pumping node and the voltage pumping node.

37.     A semiconductor memory device as claimed in claim 35 or 36, further comprising precharge means for precharging the output of said first and second pumping nodes to a predetermined voltage.

- 20     38.     A semiconductor memory device as claimed in claim 34, 35, 36 or 37, further comprising means for precharging a voltage at the voltage pumping node to a predetermined voltage.

- 25     39.     A semiconductor memory device as claimed in any of claims 34 to 38, wherein said active kicker means comprise:

         a logic combination circuit for receiving signals from the circuitry;

         a kicking node;

a pre-kicker for setting a voltage at the kicking node to a first level when the output of the logic combination circuit is at a first state;

5 a kicking driver converting the voltage at the kicking node from said first level to a second level when the output of the logic combination circuit is at a second state; and

10 a third isolation transistor with a channel connected between the kicking node and the voltage pumping node, said third isolation transistor operating in response to the voltage at the kicking node.

40. A semiconductor memory device as claimed in any of claims 34 to 39, wherein said clamping means comprise a DC current path controllable by the sensing signal, disposed in series between the pumped voltage and the supply  
15 voltage.

41. A semiconductor memory device as claimed in any of claims 34 to 39, wherein said clamping means comprise a DC current path disposed in series between the pumped voltage and the supply voltage.  
20

42. A voltage pumping circuit including voltage pumping means for supplying a pumped voltage to electrical circuitry and comprising:

25 first switching means connected between said voltage pumping means and the electrical circuitry, for supplying the pumped voltage to the electrical circuitry in response to the pumped voltage; and



second switching means comprising voltage kicking means, connected between input and output terminals of the electrical circuitry, for supplying a kicked voltage output from the voltage kicking means to the electrical circuitry in response to the output of the electrical circuitry.

5

43. A voltage pumping circuit as claimed in claim 42, wherein said first switching means comprise an insulated gate field effect MOS transistor with a gate connected to the pumped voltage and a channel connected between the pumped voltage and the electrical circuitry.

10

44. A voltage pumping circuit as claimed in claim 42 or 43, wherein said second switching means comprise an insulated gate field effect MOS transistor with a gate connected to the kicked voltage and a channel connected between the kicked voltage and the pumped voltage.

15

45. A semiconductor memory device including:  
a plurality of memory cells;

a plurality of word lines coupled to the memory cells;

20

a plurality of bit lines in pairs coupled to the memory cells;

a plurality of input/output lines coupled to the bit lines;

25

a plurality of sense amplifiers coupled to the bit line pairs, for amplifying a voltage difference between the bit lines in each pair;

a plurality of isolation gates coupled between the bit lines and the input/output lines; and

a plurality of word line drivers for selecting the word lines:

5

said semiconductor memory device further comprising:

a voltage pumping node coupled to electrical circuitry to which a pumped voltage is provided;

10

a voltage pumping circuit for generating the pumped voltage for a power-up cycle of the semiconductor memory device;

15

isolation means for supplying the pumped voltage to said voltage pumping node in response to the pumped voltage;

active kicker means for compensating for a voltage drop of the pumped voltage in response to the signal output from the electrical circuitry;

20

detecting means for feeding-back a sensing signal indicative of variation of the pumped voltage to said voltage pumping means; and

clamping means for receiving the sensing signal to clamp the pumped voltage by compensating for a voltage pull-up of the pumped voltage.

25

46. A semiconductor memory device as claimed in claim 45, wherein said voltage pumping means comprise:

an oscillator for generating a pumping clock in response to states of a supply voltage and the sensing signal; and

5 first and second charge pumps having first and second pumping nodes, said first and second charge pumps each operating complementarily in response to the pumping clock.

47. A semiconductor memory device as claimed in claim 46, wherein said isolation means comprise:

10 a first isolation transistor with a gate connected to the first pumping node and a channel connected between the first pumping node and the voltage pumping node; and

15 a second isolation transistor with a gate connected to the second pumping node and a channel connected between the second pumping node and the voltage pumping node.

48. A semiconductor memory device as claimed in claim 46 or 47, further comprising means for precharging a voltage at the first and second pumping nodes to a predetermined voltage.

20 49. A semiconductor memory device as claimed in claim 45, 46, 47 or 48, further comprising means for precharging a voltage at the voltage pumping node to a predetermined voltage.

25

50. A semiconductor memory device as claimed in any of claims 45 to 49 wherein said active kicker means comprise:

a logic combination circuit for receiving signals from the circuitry;

a kicking node;

5        a pre-kicker for setting a voltage at the kicking node to a first level  
when the output of the logic combination circuit is at a first state;

10       a kicking driver converting the voltage at the kicking node from said  
first level to a second level when the output of the logic combination circuit  
is at a second state; and

15       a third isolation transistor with a channel connected between the kicking  
node and the voltage pumping node, said third isolation transistor operating  
in response to the voltage at the kicking node.

51.    A semiconductor memory device as claimed in any of claims 45 to 50,  
wherein said clamping means comprise a DC current path controllable by the  
sensing signal, disposed in series between the pumped voltage and the supply  
voltage.

20       52.    A semiconductor memory device as claimed in any of claims 45 to 50,  
wherein said clamping means comprise a DC current path disposed in series  
between the pumped voltage and the supply voltage.

25       53.    A semiconductor memory device as claimed in any of claims 45 to 50,  
wherein said clamping means comprise:

a first clamping circuit for supplying a first voltage to the voltage pumping node if the supply voltage is identical to the first voltage; and

5 a second clamping circuit for supplying a second voltage higher than the first voltage to the voltage pumping node if the supply voltage is identical to the second voltage.

54. A voltage pumping circuit substantially as hereinbefore described with reference to any of Figures 2 to 8 of the accompanying drawings.

10

55. A semiconductor memory device provided with a voltage pumping circuit according to any of the preceding claims.

Relevant Technical fields

- (i) UK Cl (Edition L ) G4C (C700N, C11407I, C11407P,  
C11413, C1134P, C1134P7, C1134P8)
- (ii) Int Cl (Edition S ) G11C (5/14, 7/00, 11/407, 11/413,  
11/34)

Search Examiner

B J EDE

Databases (see over)

(i) UK Patent Office

(ii)

Date of Search

29 JANUARY 1993

Documents considered relevant following a search in respect of claims 1-10

Category (see over)	Identity of document and relevant passages	Relevant to claim(s)
X	EP 0030244 A1 (FUJITSU) see Figures 4-7	1 and 3
X	US 4918663 (REMINGTON ET AL) see Figure 1	1 and 3
X	US 4905199 (MIYAMOTO) see Figures 15 and 16	1 and 3
X	US 4672586 (SHIMOHIGASHI) see Figure 4	1
X	US 4455628 (OZAKI) see Figure 4	1 and 3